Chapter 3: Phase-Lock and Frequency Feedback Techniques

Figure 3-1 depicts a block diagram of a *phase-lock loop* (PLL). A considerable number of variations of this basic architecture have been proposed and used. However, many of these variants are mathematically equivalent to the loop described here. For reasons that will become clear as the topic is pursued, Figure 3-1 depicts what is often referred to as a *short loop* or a *base band model* of the PLL.

The PLL depicted by Fig. 3-1 contains 1) a phase comparator (also known as a phase detector), 2) a loop filter, and 3) a voltage controlled oscillator (VCO). The phase comparator may be a simple analog multiplier. A different, usually more complicated, phase comparator may be used to exploit attributes (like a high input signal-to-noise ratio) of a given application. When present, the loop filter is low pass in nature, and it may be active or passive. The VCO oscillates with an instantaneous frequency that is functionally related to its control voltage e.

The external reference signal supplied to the loop is modeled as the sum of a desired signal $\sqrt{2}A\sin\theta_i(t)$ and an undesired additive noise component $\eta(t)$. In addition to random noise, the output of the phase comparator contains a component that quantifies the phase error $\phi \equiv \theta_i - \theta_v$. This component is processed by the loop filter, and the results are applied to the input of the VCO. Hopefully, this controls the VCO phase and results in a small value of phase error variance.

Under phase-locked conditions in a properly designed and operated PLL, the VCO
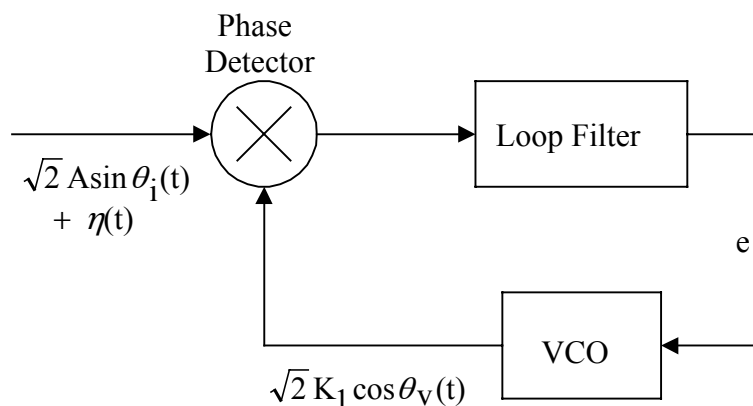

Figure 3-1: Basic phase-lock loop.

instantaneous phase θ_v remains close to the phase θ_i of the desired input signal, and the phase error $\phi(t) \equiv \theta_i(t) - \theta_v(t)$ is small in absolute value. This implies that the VCO leads the reference in phase by approximately $\pi/2$ radians. Of course, the presence of input noise η insures that θ_v and ϕ are random processes. However, in many practical applications, the PLL can be designed so that the variance of ϕ is acceptably small, and the PLL tracks well the phase θ_i of the desired input signal. In these applications, the PLL can be thought of as a filter that eliminates the bulk of the noise appearing at its input.

Phase lock is the end result of a process known as *pull in*. That is, pull in is the natural mechanism by which phase lock is achieved after starting from an out-of-lock condition. Pull in may, or may not, be possible when the loop is closed. If possible, it may not be achieved, or it may not happen in a reasonable amount of time. Often, the pull in mechanism must be aided by circuitry added to the basic PLL.

Basic Applications

The subject of phase-locked loops first generated major interest with the advent of the space program in the early 1960s. Major advances in integrated circuits since this time have brought down the cost and trouble of using PLL technology. In addition to being used in military and space applications, PLLs have been incorporated into consumer electronic products which are taken for granted by the public. Some of these applications are described in what follows.

Coherent Demodulation of Amplitude Modulated Signals

Amplitude modulated (AM) signals can be demodulated coherently by using the system depicted by Fig. 3-2. When this PLL is phase locked to the AM signal carrier component, the VCO produces a sinusoid that is in phase quadrature with the received carrier. This implies that the output of the $-90°$ phase shifter will be in phase with the signal carrier component, and that an estimate of the envelope $\sqrt{2}\,[A + m(t)]$ appears at the terminals of the output filter.

This method of AM demodulation can produce excellent results. In a noisy environment, it can produce performance which far exceeds the classical envelope detector. Of course, along
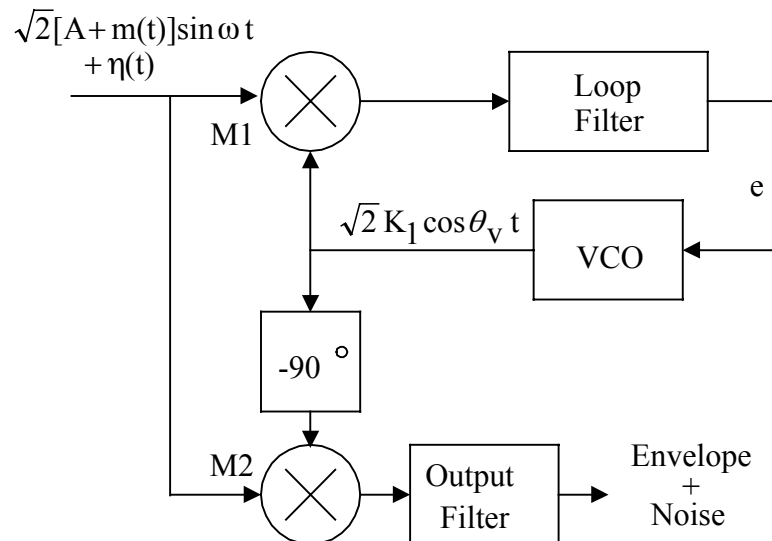
$$\sqrt{2}[A+m(t)]\sin\omega t + \eta(t)$$

$$\sqrt{2}\,K_1\cos\theta_v t$$

Figure 3-2: Coherent demodulation of AM.

with the additional performance of coherent demodulation come the additional complexity and cost. Phase-locked AM demodulators are far more complicated and expensive than simple envelope detectors. For this reason, coherent demodulation of AM is not used in most commercial broadcast receivers (AM radios).

Frequency Synthesis

The PLL plays a major role in the frequency synthesis of spectrally pure signals. Figure 3-3 depicts a block diagram of a simple PLL-based *frequency synthesizer*. As discussed below, this system is capable of generating a sinusoid at a frequency of Nf_0 Hz, where integer N is user-
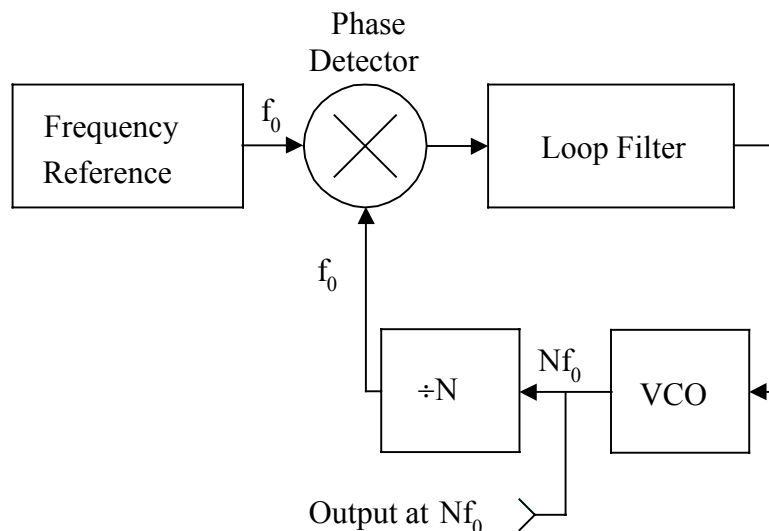

Figure 3-3: A simple PLL-based frequency synthesizer.

programmable. The frequency stability of the generated sinusoid is dependent on the stability of the reference, and it can be excellent.

In many applications, the reference signal at f_0 Hz is obtained from a digital counter (frequency divider) circuit driven by a highly stable crystal oscillator. Hence, the phase comparator is fed digital signals in this application. Specialized phase comparators are used which exploit the noise-free nature of the signals involved. Often the phase comparator is augmented by a frequency comparator that helps the loop achieve a stable phase-lock state.

The VCO oscillates at Nf_0 Hz when the synthesizer is phase locked. Since N is user-programmable, this system can generate a wide range of frequencies at a basic resolution of f_0 Hz. In many applications, it is possible to do this while maintaining adequate frequency stability, spectral purity and switching times of the synthesized output signal.

Demodulation of BPSK Signals

Binary phase shift keying (BPSK) is a popular form of modulation which is used in the transmission of digital information. Let d(t) denote a binary ($\pm A$ volts) waveform representing digital information. The BPSK modulator forms the signal $d(t)\cos\omega_0 t$; in applications, carrier frequency ω_0 is much higher than the rate of the clock used to generate d(t) (often, ω_0 is an integer multiple of the data clock frequency).

In many applications, data signal d(t) is constructed to have an average value of zero. Usually, this is accomplished by constructing the data signal from specially formulated binary symbols that have an average value of zero. A zero average value for d(t) is desirable from an efficiency standpoint; it insures that the transmitted signal has no carrier component at ω_0, and all of the transmitted power appears in the sidebands where it is used to convey information.

At the receiver, efficient demodulation of the BPSK signal requires the use of a sinusoid that is phase coherent with the suppressed carrier. This sinusoid can be generated by the *squaring loop* depicted by Fig. 3-4. First, the received signal is squared to produce a second signal that has a strong component at $2\omega_0$. The band pass filter (BPF) passes this $2\omega_0$ component, and it attenuates all other frequency components. The PLL locks on the $2\omega_0$
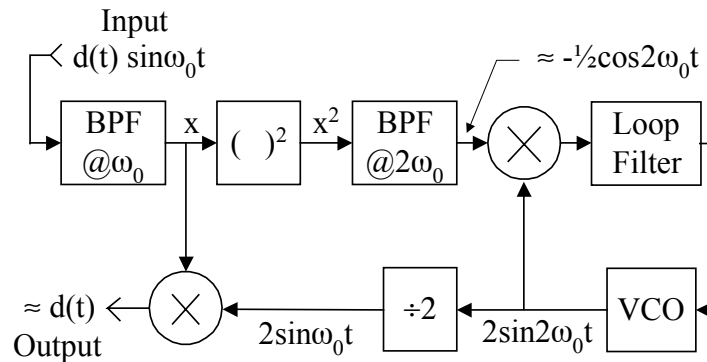
Figure 3-4: Squaring loop data demodulator.

frequency component found in the BPF output. In this role, the PLL acts like a narrow band filter centered at $2\omega_0$. A digital counter is used to divide by two the frequency of the VCO. This division operation produces a signal that is phase coherent with the suppressed carrier of the received signal. Finally, this locally generated reference signal is used to demodulate the received signal and produce an estimate of data d(t).

Phase-Locked Receivers

There are many applications which require the reception of a Doppler shifted signal. Often, the amount of Doppler shift is changing with time, and there is a large amount of uncertainty in the received signal frequency. One possible solution to the problem of receiving this signal is to use a non-coherent approach based on a wide bandwidth receiver that can "hear" the signal regardless of the Doppler shift. However, this simple approach may bear a significant noise penalty since received noise power is proportional to receiver bandwidth. Large Doppler shifts would require large receiver bandwidths, and large bandwidths would lead to large amounts of received noise power and poor system performance.

A *phase-locked receiver* is a better solution to the problem of receiving a Doppler shifted signal. The receiver electronically tunes itself so that it tracks out Doppler on the received signal. Hence, such a receiver can have a bandwidth that is comparable to the signal, so no noise penalty has to be paid to accommodate the unknown carrier frequency of the signal. In most cases, a solution based on a tracking receiver will be substantially better than that afforded by the above-mentioned scheme that utilizes a wide bandwidth, fixed frequency receiver.
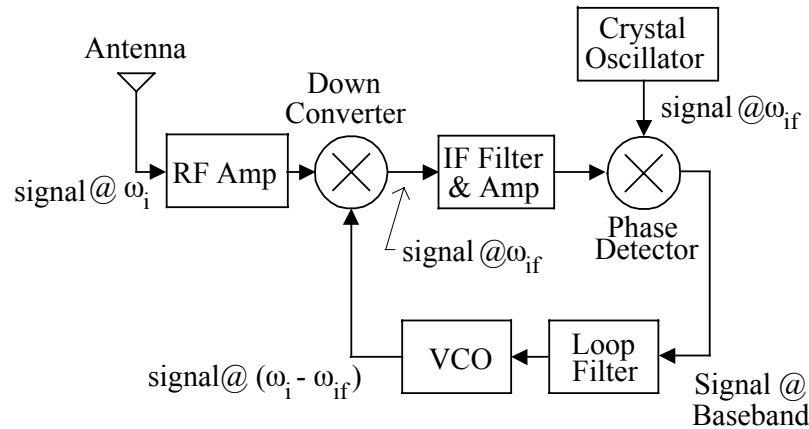
Figure 3-5: Simplified block diagram of a phase-locked receiver.

Figure 3-5 depicts a simplified block diagram of a tracking phase-locked receiver. In the PLL literature, this architecture is known as a *long-loop*. Note that most of the receiver is in the feedback path; this feature reduces practical problems that can result from noise rectification in an imperfect phase comparator. Practical phase detectors are limited in dynamic range, and this limitation (known as the *phase comparator threshold problem*) is a major reason for using an intermediate frequency (IF) path within the loop. It can be shown that the PLL depicted by Fig. 3-5 is mathematically equivalent to a short loop of the type illustrated by Fig. 3-1.

Normally, the receiver locks to the carrier frequency of the received signal. As the carrier frequency changes due to Doppler, the VCO is tuned automatically by loop dynamics so that the output of the down converter remains within the IF pass band. In many practical applications, the *rate* of Doppler change is small (even if the total amount of Doppler is large), and the overall bandwidth of the closed loop may be on the order of a few tens of Hz.

For example, consider an S-band (2.4 GHz) satellite in low earth orbit. Suppose that the satellite is transmitting a carrier that a ground station must recover. Depending on the particular overhead pass, the satellite downlink signal may contain as much as ±70 kHz of Doppler as seen by the ground station. Without Doppler tracking abilities, the wide band receiver at the ground station would need a bandwidth of 140 kHz. However, in this application, the rate of change in Doppler is moderate to small, and the satellite signal could be received by a PLL-based Doppler tracking receiver that utilizes a bandwidth on the order of 10 Hz.

Received noise power is directly proportional to receiver bandwidth. For the example outlined above, it turns out that the fixed-frequency, wide band receiver approach would pay a signal-to-noise ratio penalty of approximately 42 dB as compared to the phase-locked receiver. Penalties of this magnitude cannot stand; this is why narrow band, phase-locked, tracking receivers are used in almost all applications involving earth-orbiting satellites.

The phase-locked receiver depicted by Figure 3-5 is based on what is called a *long loop*. The distinguishing characteristic of a long loop is that it contains an intermediate frequency (IF) signal path; an example of such a loop is illustrated by Fig. 3-6. The received signal is heterodyned twice in order to form the base band signal x(t) that drives the loop filter. First, the VCO output is used to heterodyne the received signal down to a band pass IF signal $x_{bp}(t)$ at an IF frequency of ω_{if}; then, x_{bp} is passed through an IF filter/amplifier to produce $y_{bp}(t)$. Next, the output of a crystal oscillator at ω_{if} is used to heterodyne y_{bp} down to the base band signal x(t) that drives the loop filter. On Fig. 3-6, constant γ appears as an arbitrary phase angle in the crystal oscillator output. In what follows, this long loop is shown to be mathematically equivalent to a base band, or short, loop (*i.e.*, one that does not containing an IF signal path).

While the two loop architectures (*i.e.*, long and short loops) are mathematically equivalent, the long loop implementation is preferred in practical applications where the desired
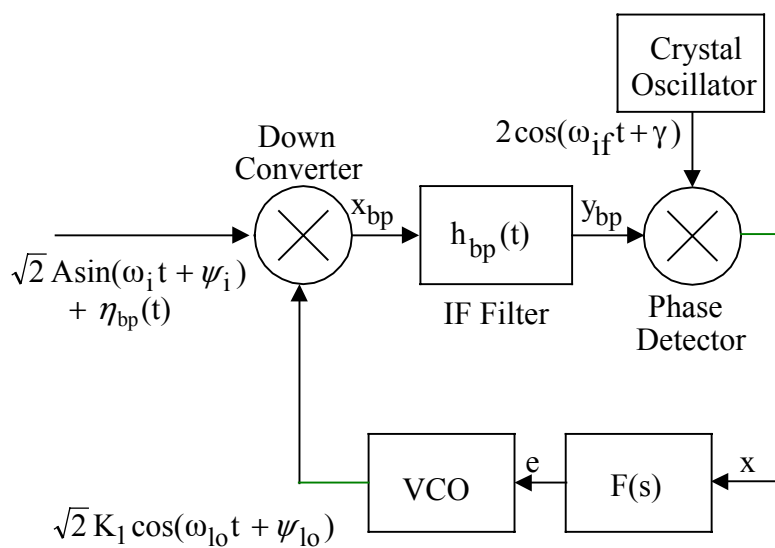

Figure 3-6: A long loop containing an IF signal path.

input reference signal is swamped in wide band noise (on Fig. 3-6, η_{bp} represents wide band noise). The reason for this is that a real phase comparator is imperfect; it has a finite dynamic range, and it exhibits a threshold phenomenon due to rectification of the input noise. Substantial wide band noise power applied on the phase comparator input could cause a DC component to appear at its output. This noise rectification-induced DC component could dominate the desired DC component due to normal operation of the loop. The occurrence of this phenomenon could degrade the signal acquisition and tracking abilities of the PLL.

This problem is minimized by using the long loop architecture depicted by Fig. 3-6. Of course, there is still the potential for noise rectification in the first down converter shown on this figure. However, the resulting DC component in x_{bp} would be rejected by the IF filter. This IF filter serves to minimize the effects of noise rectification by limiting the total noise power that reaches an imperfect phase comparator.

Base Band Model of the Long Loop

In this section, a base band model of the loop depicted by Fig. 3-6 is developed. To simplify the analysis, it is assumed that the input reference is noise free (set $\eta_{bp} = 0$ on Fig. 3-6). Of course, this assumption in no way influences the base band architecture.

The output of the down converter on Fig. 3-6 is given by

$$x_{bp} = AK_1 \sin(\omega_{if}\, t + \psi_{if}) \qquad\qquad\qquad (3\text{-}1)$$

where $\omega_{if} \equiv \omega_i - \omega_{lo}$, and $\psi_{if} \equiv \psi_i - \psi_{lo}$. Here it is assumed that low-side injection is used so that $\omega_i > \omega_{lo}$. Also, the sum frequency term in x_{bp} is omitted since it is rejected by the IF filter. Finally, note that x_{bp} can be written as

$$x_{bp} = x_c(t)\cos(\omega_{if}\,t) - x_s(t)\sin(\omega_{if}\,t)$$

$$x_c(t) \equiv AK_1 \sin(\psi_{if}) \tag{3-2}$$

$$x_s(t) \equiv -AK_1 \cos(\psi_{if}).$$

In what follows, low pass equivalent signals are used to analyze the IF path and find the base band signal x(t) in the long loop depicted by Fig. 3-6. IF signal x_{bp} can be represented as $x_{bp} = \mathrm{Re}[x_{lp}\exp(j\omega_{if}\,t)]$, where

$$x_{lp} = x_c + j\,x_s \tag{3-3}$$

is its low pass equivalent. The band pass IF filter $h_{bp} = \mathrm{Re}[h_{lp}\exp(j\omega_{if}\,t)]$ in Fig. 3-6 is assumed to be symmetrical. This means that it has a real-valued low pass equivalent

$$h_{lp} = h_c. \tag{3-4}$$

The low pass equivalent y_{lp} of band pass output y_{bp} is

$$y_{lp} = \frac{1}{2}x_{lp}*h_{lp} = \frac{1}{2}(x_c + j\,x_s)*h_c, \tag{3-5}$$

so that the band pass output of the IF filter can be expressed as

$$y_{bp} = \frac{1}{2}\mathrm{Re}\big[\,[(x_c + j\,x_s)*h_c]\exp(j\omega_{if}\,t)\,\big]. \tag{3-6}$$

Now, the phase detector depicted on Fig. 3-6 forms the product

$$y_{bp}\cdot 2\cos(\omega_{if}\,t+\gamma) = \frac{1}{2}\mathrm{Re}\big[\,[(x_c + j\,x_s)*h_c]\exp(j\omega_{if}\,t)2\cos(\omega_{if}\,t+\gamma)\,\big] \tag{3-7}$$

of y_{bp} and the output of the crystal oscillator. To simplify this last result note that

$$\exp(j\omega_{if}t)2\cos(\omega_{if}t+\gamma) = \exp[j(2\omega_{if}t+\gamma)]+\exp(-j\gamma), \qquad (3\text{-}8)$$

and the base band component in this product is the constant $e^{-j\gamma}$. Hence, on Fig. 3-6, the base band component in the output of the phase detector is

$$x = \frac{1}{2}\text{Re}\left[[(x_c+jx_s)*h_c]e^{-j\gamma} \right], \qquad (3\text{-}9)$$

a result obtained from inspection of (3-7) and (3-8).

The IF signal path on Fig. 3-6 can be removed by realizing that the IF filter/phase comparator combination can be replaced by a phase comparator followed by a scaled version of the low pass equivalent of the IF filter. To see this, note that the product of x_{bp} and $2\cos(\omega_{if}t + \gamma)$ can be written as

$$x_{bp}\cdot 2\cos(\omega_{if}t+\gamma) = \text{Re}\left[[(x_c+jx_s)\exp(j\omega_{if}t)2\cos(\omega_{if}t+\gamma) \right], \qquad (3\text{-}10)$$

which has a base band component given by

$$\text{Re}[(x_c+jx_s)e^{-j\gamma}]. \qquad (3\text{-}11)$$

As can be seen from (3-9), the base band signal x results if (3-11) is passed through low pass ½h_c. Hence, parts a) and b) of Fig. 3-7 depict mathematically equivalent methods of generating base band x. However, the two successive down conversions shown on Fig. 3-7b produce
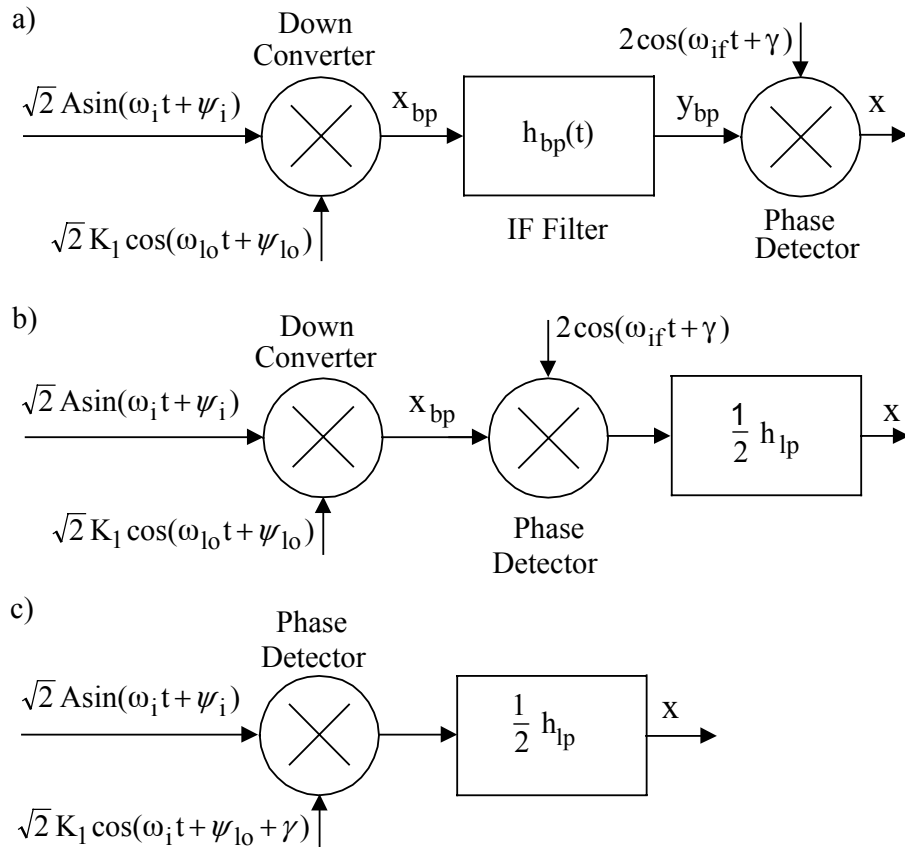
a)

b)

c)

Figure 3-7: Three mathematically equivalent ways of producing base band signal x.

$$\sqrt{2}\,A\sin(\omega_i t + \psi_i)\sqrt{2}\,K_1\cos(\omega_{lo} t + \psi_{lo})2\cos(\omega_{if}\,t + \gamma)\,, \qquad (3\text{-}12)$$

and the base band component of this product is filtered by $\tfrac{1}{2}h_{lp}$. But, the base band component in

$$\sqrt{2}\,A\sin(\omega_i t + \psi_i)\sqrt{2}\,K_1\cos(\omega_i t + \psi_{lo} + \gamma) \qquad (3\text{-}13)$$

is identical to the one in (3-12), so Fig. 3-7c is mathematically equivalent to parts a) and b) of this diagram. Finally, this last observation implies that Fig. 3-8 depicts a base band PLL which is equivalent to the long loop illustrated by Fig. 3-6. On Fig. 3-8, the VCO has a center frequency that exceeds by ω_{if} the center frequency of the VCO depicted on Fig. 3-6.
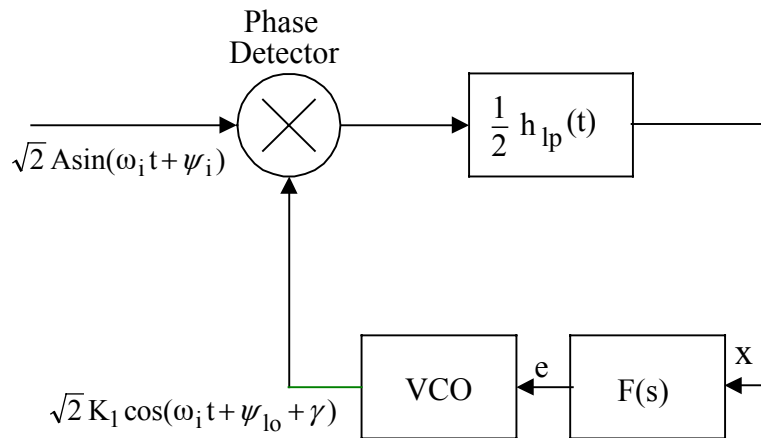
Figure 3-8: A base band loop equivalent to the long loop.

As mentioned above, the IF filter serves to limit the broad band noise power that reaches the phase detector. The goal of the IF filter is to limit the undesirable side effects that can occur when an imperfect phase detector is swamped with noise. To a satisfactory degree, this goal can be accomplished in many applications with an IF filter bandwidth that is large compared to the overall closed loop bandwidth. In these cases, a common perception is that the IF filter only has a minor influence on the dynamics of the closed loop. However, this perception may not be true in practical applications. The "small" effects of an IF filter can limit the pull-in range and cause other unacceptable behavior.

Modeling the PLL's Analog Phase Detector

A noiseless reference signal is used to drive the PLL depicted by Fig. 3-9. The phase
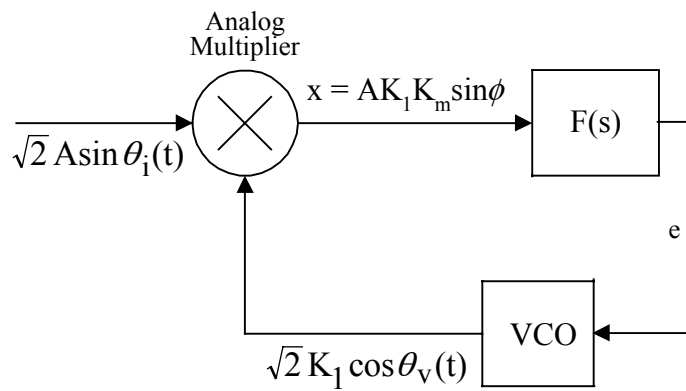

Figure 3-9: PLL with a noiseless reference signal.

comparator used here is a simple analog multiplier with output

$$x \equiv K_m[\sqrt{2}\,A\sin\theta_i][\sqrt{2}\,K_1\cos\theta_v] = AK_1K_m[\sin(\theta_i - \theta_v) + \sin(\theta_i + \theta_v)]. \qquad (3\text{-}14)$$

The quantity K_m is the phase comparator gain; as discussed in what follows, it has units of volts/radians.

The sum frequency term $AK_1K_m\sin(\theta_i + \theta_v)$ in (3-14) is considered to be a band pass process centered around twice the input reference frequency. In most applications, it is filtered out by the combination of loop filter and VCO. Hence, this sum frequency term is discarded in what follows, and the phase comparator output is approximated as

$$x = AK_1K_m\sin(\phi), \qquad (3\text{-}15)$$

where

$$\phi \equiv \theta_i - \theta_v. \qquad (3\text{-}16)$$

The quantity ϕ plays a prominent role in PLL analysis; it is known as the *closed loop phase error*.

Modeling the PLL's Loop Filter

The error signal $x = AK_1K_m\sin\phi$ shown on Fig. 3-9 drives the linear, time-invariant loop filter to produce the VCO control voltage e. The relationship between the error signal and control voltage can be given in both the Laplace and time domains as is summarized by Fig. 3-10.

In the Laplace domain, the filter can be described by the transfer function

x → [Loop Filter] → e

(a) $\qquad \mathscr{L}[e] = \dfrac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_0} \mathscr{L}[x]$

(b) $\qquad \left[b_n \dfrac{d^n}{dt^n} + b_{n-1} \dfrac{d^{n-1}}{dt^{n-1}} + \cdots + b_0 \right] e = \left[a_m \dfrac{d^m}{dt^m} + a_{m-1} \dfrac{d^{m-1}}{dt^{m-1}} + \cdots + a_0 \right] x$

(c) $\qquad e(t) = \displaystyle\int_0^t f(u) x(t-u)\, du + e_0(t)$

Figure 3-10: Laplace domain description of loop filter is given by a). Time domain descriptions are given by b) and c).

$$F(s) = \dfrac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_0}, \quad m \le n, \qquad\qquad (3\text{-}17)$$

where integer n denotes filter order. This rational function of s is the ratio of filter output to input in the Laplace domain. In practical PLLs, Equation (3-17) has no poles in the right half of the s-plane.

In the time domain, the nth-order differential equation

$$L_1[e] = L_2[x]$$

$$L_1 \equiv b_n \dfrac{d^n}{dt^n} + b_{n-1} \dfrac{d^{n-1}}{dt^{n-1}} + \cdots + b_0 \qquad\qquad (3\text{-}18)$$

$$L_2 \equiv a_m \dfrac{d^m}{dt^m} + a_{m-1} \dfrac{d^{m-1}}{dt^{m-1}} + \cdots + a_0$$

defines the loop filter. This equation is linear, and it has constant coefficients. Furthermore, it has a unique solution e(t), $t \ge 0$, once initial conditions

$$e(0) = e_0$$

$$\left.\frac{d^k e}{dt^k}\right|_{t=0} = e_k, \ 1 \le k \le n-1, \tag{3-19}$$

are specified.

A second time-domain relationship can be specified between the loop filter input and output. For $t \ge 0$, this relationship is

$$e(t) = \int_0^t x(\tau) f(t-\tau) d\tau \ + \ e_0(t) = \int_0^t x(t-\tau) f(\tau) d\tau \ + \ e_0(t), \tag{3-20}$$

where

$$f(t) \equiv \mathcal{L}^{-1}[F(s)] \tag{3-21}$$

is the filter impulse response. In (3-20), $e_0(t)$ is the zero-input response which depends only on initial conditions existing in the circuit at $t = 0$.

Modeling the PLL's Voltage Controlled Oscillator

The VCO accepts as input the error control voltage e and produces as output the sinusoidal signal $\sqrt{2}\, K_1 \cos\theta_v$. The commonly-used VCO model relates variables θ_v and e by

$$\frac{d\theta_v}{dt} = \omega_0 + K_v e, \tag{3-22}$$

where ω_0 and K_v are known constants. As can be seen from inspection of (3-22), the VCO oscillates at frequency ω_0 radians/second when its input control voltage e is set to zero. Hence, ω_0 is known as the VCO *center*, or *quiescent frequency*. The frequency of the VCO oscillation changes by K_v radians/second for every volt of control signal e applied as input. Hence, K_v is
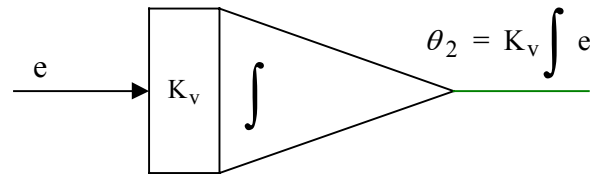
Figure 3-11: Model of the VCO as an integrator.

known as the *VCO gain parameter*, and it has units of radians/second-volt.

The analysis of the PLL is simplified by defining input reference and VCO phase variables which are relative to the VCO quiescent phase $\omega_0 t$. The quantities

$$\theta_1(t) \equiv \theta_i(t) - \omega_0 t \tag{3-23}$$

$$\theta_2(t) \equiv \theta_v(t) - \omega_0 t \tag{3-24}$$

are relative input reference and VCO phases, respectively. From a modeling standpoint, relative phase θ_2 is considered as the VCO output even though a sinusoid is the physical output of this oscillator. Finally, note that closed loop phase error can be expressed in terms of these relative phase variables as $\phi = \theta_1 - \theta_2$.

With the aid of (3-22) and (3-24), it is easy to model the VCO as an integrator. Substitute (3-24) into (3-22) and obtain

$$\frac{d\theta_2}{dt} = K_v e, \tag{3-25}$$

a result depicted by Fig. 3-11. Note that the VCO response θ_2 falls off at a rate that is inversely proportional to the frequency of forcing function e. This, and the low pass nature of F(s), imply that undesired high frequency signals in the phase detector output tend to have minimal influence on the PLL.

Modeling the Nonlinear PLL

The component descriptions developed above are used in what follows to create a simple

block diagram depicting a nonlinear model of the PLL. Two approaches are discussed for mathematically describing this model. First, the model is described by an $(n+1)^{th}$-order ordinary differential equation. Next, an n+1 dimensional first-order system is used to describe the model.

PLL Description Based on an Ordinary Differential Equation

The PLL loop filter processes the phase comparator output $x = AK_1K_m\sin\phi$ to produce voltage e that drives the VCO. The nth-order differential equation

$$L_1[e] = AK_1K_mL_2[\sin\phi], \qquad\qquad (3\text{-}26)$$

obtained by combining (3-15) and (3-18), describes this processing function.

Equation (3-26) contains the dependent variables ϕ and e. A second independent relationship must be obtained between these variables to complete the nonlinear dynamical model of the PLL. This required second equation can be derived by combining (3-25) with (3-16). This effort produces the results

$$\frac{d\phi}{dt} = \frac{d\theta_1}{dt} - K_v\, e = \left[\frac{d\theta_i}{dt} - \omega_0\right] - K_v\, e\,. \qquad\qquad (3\text{-}27)$$

Equations (3-26) and (3-27) describe the closed loop dynamics of the PLL under consideration. They can be combined to produce

$$L_1\left[\frac{d\phi}{dt} - \frac{d\theta_1}{dt}\right] = -G\, L_2[\sin\phi]\,, \qquad\qquad (3\text{-}28)$$

where

$$G \equiv AK_1K_mK_v \qquad\qquad (3\text{-}29)$$

is a closed loop gain constant, and L1, L2 are differential operators given by (3-18). Constant G is assumed to be positive (if $G < 0$, perform the transformation $\phi = \pi + \tilde{\phi}$, and take G as positive). Because of the dependence on $\sin\phi$, Equation (3-28) is a nonlinear differential equation. It is autonomous (time-invariant) since only multiplicative constants appear in the equation, and it is of order n+1.

The block diagram depicted by Fig. 3-12 describes the nonlinear PLL model under consideration. Equations (3-15) and (3-16), which describe the phase detector, are implemented by the summing junction and the block containing the nonlinear operation $AK_1K_m\sin(\cdot)$. The loop filter block implements the linear transformation described by Fig. 3-10. Finally, with a gain of K_v, the VCO block integrates the control voltage e to form the relative phase angle θ_2 defined by (3-24).

PLL Description Based on a First-Order Nonlinear System

Equation (3-28) can be written as a first-order system. Define the n+1 dimensional vector

$$\vec{X} = \begin{bmatrix} x_1 & x_2 & \cdots & x_{n+1} \end{bmatrix}^T = \begin{bmatrix} \phi & \dfrac{d\phi}{dt} & \dfrac{d^2\phi}{dt^2} & \cdots & \dfrac{d^n\phi}{dt^n} \end{bmatrix}^T . \tag{3-30}$$

Then (3-28) can be used to write

$$\frac{d\vec{X}}{dt} = C\vec{X} - G\vec{F}(\vec{X}) + \vec{G} , \tag{3-31}$$

where C is the (n+1)×(n+1) constant matrix

$$L_1 = b_n \frac{d^n}{dt^n} + b_{n-1} \frac{d^{n-1}}{dt^{n-1}} + \cdots + b_0 \qquad \theta_1 = \theta_i - \omega_0 t$$

$$L_2 = a_m \frac{d^m}{dt^m} + a_{m-1} \frac{d^{m-1}}{dt^{m-1}} + \cdots + a_0 \qquad \theta_2 = \theta_v - \omega_0 t$$
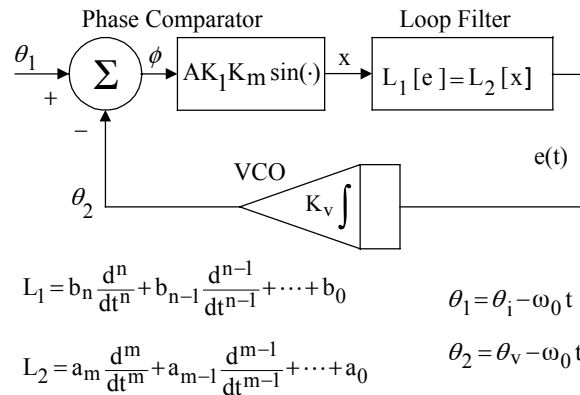
Figure 3-12: Nonlinear time domain model depicting the function of each component.

$$C \equiv \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ 0 & -b_0/b_n & -b_1/b_n & \cdots & -b_{n-1}/b_n \end{bmatrix}, \qquad (3\text{-}32)$$

and $\vec{\mathbf{F}}$, $\vec{\mathbf{G}}$ are the n+1 vectors

$$\vec{\mathbf{F}}(\vec{\mathbf{X}}) = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & b_n^{-1} L_2[\sin x_1] \end{bmatrix}^T$$

$$\vec{\mathbf{G}} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & b_n^{-1} L_1\left[\frac{d\theta_1}{dt}\right] \end{bmatrix}^T. \tag{3-33}$$

Equation (3-31) is an n+1 dimensional, nonlinear system that describes the PLL.

Modeling the Linear PLL

      Consider the case when the PLL is phase locked, and phase error ϕ is small in absolute value. Under this condition, the approximation $\sin\phi \approx \phi$ can be made, and the PLL model can be linearized. The linear loop can be described by the Laplace domain model depicted by Fig. 3-13; the variables
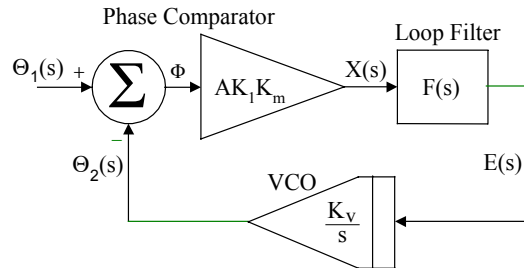
Figure 3-13: Linear Laplace domain model showing the function of each component.

$$\Theta_1(s) \equiv \mathscr{L}[\theta_1(t)]$$

$$\Theta_2(s) \equiv \mathscr{L}[\theta_2(t)]$$

$$\Phi(s) \equiv \mathscr{L}[\phi(t)]$$

$$E(s) \equiv \mathscr{L}[e(t)]$$

(3-34)

are employed in the Laplace domain model.

      A transfer function H(s) can be obtained that relates output Θ_2 to input Θ_1. From inspection of Fig. 3-13, the open loop transfer function is

$$G_0(s) \equiv \frac{\Theta_2(s)}{\Phi(s)} = G\left[\frac{F(s)}{s}\right] \quad , \tag{3-35}$$

where closed loop gain constant G is given by (3-29). This open-loop transfer function can be used to express Θ_2 as

$$\Theta_2(s) = G_0(s)\Phi(s). \tag{3-36}$$

Now, substitute $\Phi = \Theta_1 - \Theta_2$ into (3-36) and solve for

$$H(s) \equiv \frac{\Theta_2(s)}{\Theta_1(s)} = \frac{G_0(s)}{1 + G_0(s)} = \frac{G\,F(s)}{s + G\,F(s)}. \tag{3-37}$$

As given by (3-37), H(s) is the closed loop transfer function of the linearized PLL. This transfer function is used extensively in the practical design of PLL circuitry. Since F(s) is low pass in nature, the closed-loop transfer function H(s) is low pass, and it has a unity DC gain (H(0) = 1). Also, for sufficiently high frequencies, $|H(j\omega)|$ rolls off at 20dB per decade (if n = m) or faster (if m < n).

The poles of H(s) are the roots of

$$s \ + \ G\,F(s) = 0\,. \hspace{5cm} (3\text{-}38)$$

Stability of the linear PLL model requires that these poles be in the left half of the complex plane. The stability issue can be studied by examining the loci of poles as *G* varies from zero to infinity. Examples of these *root locus* plots are considered below. The PLL is said to be *unconditionally stable* if, for all *G* > 0, the roots of (3-38) remain in the left-half of the s-plane.

As long as the phase error remains small, transfer function H(s) and standard linear system theory can be used to determine the PLL response to any input. This is accomplished by using the relationship

$$\Theta_2(s) = H(s)\,\Theta_1(s) \hspace{5cm} (3\text{-}39)$$

to find the Laplace transform of the output given an input Θ_1. Then, time domain output $\theta_2(t)$ can be calculated by computing the inverse transform of Θ_2.

The linear theory can be used to determine the closed loop phase error. This is accomplished by using (3-39) with $\Phi = \Theta_1 - \Theta_2$ to obtain

$$\Phi = \Theta_1 - H\,\Theta_1 = (1 - H)\Theta_1\,. \hspace{4cm} (3\text{-}40)$$

Alternatively, the linear analysis can be carried out in the time domain with the use of

$$h(t) \equiv \mathcal{L}^{-1}[H(s)], \tag{3-41}$$

the impulse response of the closed loop. For $t \geq 0$, the zero-state response for a given input $\theta_1(t)$ can be expressed by the convolution

$$\theta_2(t) = \int_0^t h(t-\tau)\, \theta_1(\tau)\, d\tau, \tag{3-42}$$

and the closed loop phase error can be expressed as

$$\phi(t) = \theta_1(t) - \int_0^t h(t-\tau)\, \theta_1(\tau)\, dt. \tag{3-43}$$

These results assume that input $\theta_1(t)$ is applied at $t = 0$, and all initial conditions are zero (θ_2 and its derivatives are zero at $t = 0^-$).

Modeling a PLL with an Angle Modulated Reference Source

         Consider the PLL depicted by Fig. 3-1 with an angle modulated reference centered at a frequency of ω_i. This reference signal is described in this section, and it can represent a frequency modulated (FM) or phase modulated (PM) signal. Assume that the loop is phase locked and that the phase error remains small for all time so that the linear model can be used.

         For the case under consideration the reference phase can be expressed as

$$\theta_i(t) = \omega_i t + \chi(t), \tag{3-44}$$

where χ depends linearly on message m(t). This implies that

$$\theta_1(t) = \omega_\Delta t + \chi(t), \tag{3-45}$$

where $\omega_\Delta \equiv \omega_i - \omega_0$ is known as the *loop detuning parameter*. For the case of phase modulation (PM), message-dependent function χ is given by

$$\chi(t) = K_p \, m(t), \tag{3-46}$$

where K_p is the modulation index with units of radians/volt. For the case of frequency modulation (FM), function χ is

$$\chi(t) = K_f \int_0^t m(t) \, dt, \tag{3-47}$$

where modulation index K_f has units of radians/second-volt.

     A simple case of practical importance has $m(t)$ as a sinusoid of frequency ω_m, and the sinusoidal steady-state loop response is desired. To unify the treatment of the two types of modulation during the solution of this problem, assume that

$$m(t) = \begin{cases} A_m \sin \omega_m t & \text{for PM} \\ A_m \cos \omega_m t & \text{for FM} \end{cases}. \tag{3-48}$$

Then, for both cases

$$\chi(t) = \beta \sin(\omega_m t), \tag{3-49}$$

where

$$\beta = \begin{cases} A_m K_p & \text{for PM} \\ \dfrac{A_m K_f}{\omega_m} & \text{for FM} \end{cases}, \tag{3-50}$$

so that

$$\theta_1(t) = \omega_\Delta t + \beta \sin \omega_m t .\tag{3-51}$$

The steady-state loop response can be obtained by substituting (3-51) into (3-42) and considering the limiting form of the results as time becomes large. The first of these steps yields

$$\theta_2 = \int_0^t h(t-\tau)\omega_\Delta \tau \, d\tau + \int_0^t h(t-\tau)\beta \sin(\omega_m \tau) \, d\tau .\tag{3-52}$$

The second integral on the right-hand side is the response of a linear system to a sinusoid at frequency ω_m. The steady-state form of this response is

$$\beta \left| H(j\omega_m) \right| \sin(\omega_m t + \angle H(j\omega_m)),\tag{3-53}$$

where $\left| H(j\omega_m) \right|$ and $\angle H(j\omega_m)$ represent the magnitude and phase, respectively, of the system at ω_m. Through a simple change of variable, the first integral on the right-hand side of (3-52) can be expressed as

$$\omega_\Delta \int_0^t (t-\tau) h(\tau) \, d\tau = \omega_\Delta \left[t \int_0^t h(\tau) \, d\tau - \int_0^t \tau \, h(\tau) \, d\tau \right].\tag{3-54}$$

Now, as time becomes large, the limiting form of (3-54) follows from the observation that

$$\begin{aligned} &\lim_{t\to\infty} \int_0^t h(\tau) \, d\tau = H(s) \Big|_{s=0} = 1 \\ &\lim_{t\to\infty} \int_0^t \tau \, h(\tau) \, d\tau = -\frac{dH(s)}{ds} \Big|_{s=0} = \left[G F(0) \right]^{-1}. \end{aligned}\tag{3-55}$$

Hence, the first integral on the right-hand side of (3-52) produces the component

$$\omega_\Delta t \ - \ \frac{\omega_\Delta}{G\,F(0)} \tag{3-56}$$

in the steady state. Finally, combine (3-53) and (3-56) to produce

$$\theta_2(t) = \omega_\Delta t \ - \ \frac{\omega_\Delta}{G\,F(0)} \ + \ \beta\left|H(j\omega_m)\right|\sin(\omega_m t \ + \ \angle H(j\omega_m)) \tag{3-57}$$

as the steady-state response of the linear model to a sinusoidally-modulated reference.

The sinusoidal steady-state phase error can be found by using (3-57) with (3-51). The result of this combination is

$$\phi(t) = \ \frac{\omega_\Delta}{G\,F(0)} \ + \ \beta\left[\sin\omega_m t \ - \ \left|H(j\omega_m)\right|\sin(\omega_m t \ + \ \angle H(j\omega_m))\right]. \tag{3-58}$$

Note that the average value of the phase error is inversely proportional to $GF(0)$, the open-loop DC gain. Also, note from (3-37) that $\left|H(j\omega_m)\right|$ and $\angle H(j\omega_m)$ approach unity and zero, respectively, as ω_m approaches zero. This implies that, as ω_m decreases (for ω_m well within the closed-loop bandwidth), the sinusoidal component in (3-58) becomes small, and the PLL tracks the modulation very well. Conversely, as ω_m becomes large (for ω_m well outside the closed-loop bandwidth), the sinusoidal component of the phase error approaches $\beta\sin\omega_m t$, and the PLL tracks the input modulation poorly.

Consider (3-58) applied to a first-order loop. For this case, $H(s) = G/(s+G)$ and we have

$$\phi(t) = \frac{\omega_\Delta}{G} \ + \ \beta\left[\sin\omega_m t \ - \ \frac{G}{\sqrt{G^2 + \omega_m^2}}\sin\left(\omega_m t \ - \ \tan^{-1}(\omega_m/G)\right)\right]. \tag{3-59}$$

For ω_m well within closed-loop bandwidth G, $\phi \approx \omega_\Delta/G$ and the loop tracks the angle-modulated

input very well (there is almost no sinusoidal component in the phase error). However, for ω_m well outside of the closed-loop bandwidth G, $\phi \approx \omega_\Delta/G + \beta\sin\omega_m t$ and the loop tracks the angle-modulated input very poorly (in the phase error, there is as much sinusoidal component as there is on the input angle-modulated signal).

As a second example of a PLL's response to an angle-modulated reference, consider the first-order PLL and input angle modulation θ_1 that is depicted by Fig. 3-14. To simplify this problem, we assume that the input reference has a center frequency of ω_0, identical to the center frequency of the VCO. We want to determine one period of the T_m-periodic, steady-state closed loop phase error.

To obtain the steady-state response, we must first obtain the equation that describes $\phi(t)$. From

$$\frac{d\theta_v}{dt} = \omega_0 + K_v e$$

$$e = AK_1K_m \sin\phi \qquad\qquad\qquad (3\text{-}60)$$

$$\phi = (\omega_0 t + \theta_1) - \theta_v \; ,$$

we obtain the desired describing equation

$$\sqrt{2}\,A\sin(\omega_0 t + \theta_1)$$

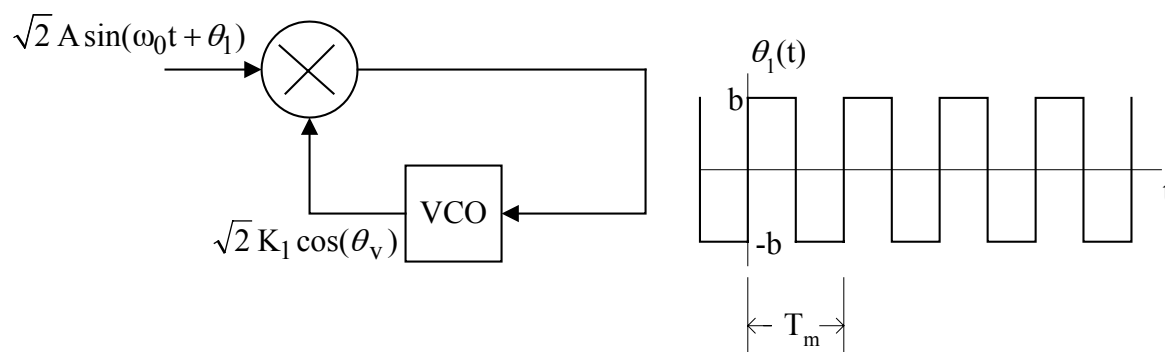$$\sqrt{2}\,K_1\cos(\theta_v)$$

Fig. 3-14: A first-order PLL with an angle modulated reference. The modulating signal is a T_m-periodic square wave $\theta_1(t)$.

$$\frac{d\phi}{dt} = \frac{d\theta_1}{dt} - G\sin\phi, \tag{3-61}$$

where $G = AK_1K_mK_v$ is the closed-loop gain. Now, if phase error ϕ remains small in magnitude, we can make linear ("linearize") (3-61) to obtain

$$\frac{d\phi}{dt} = \frac{d\theta_1}{dt} - G\phi. \tag{3-62}$$

The VCO integrates $e = AK_1K_m\sin\phi$ to form θ_v. Since error control voltage e does not contain any impulse functions, we can conclude that $\theta_v(t)$ is a continuous function of time t. Hence, every time input $\theta_1(t)$ jumps by $\pm 2b$, we must have a $\pm 2b$ jump in phase error $\phi(t)$. Also, when $\theta_1(t)$ is constant, Equation (3-62) tells us that $\phi(t)$ decays exponentially with a time constant of $1/G$. As a result, we should expect that one period of steady-state $\phi(t)$ looks like the dashed-line plot depicted on Fig. 3-15 (this plot shows one period of input $\theta_1(t)$ and one period of the steady-state phase error $\phi(t)$). All that remains is for us to determine the constant ϕ_0.
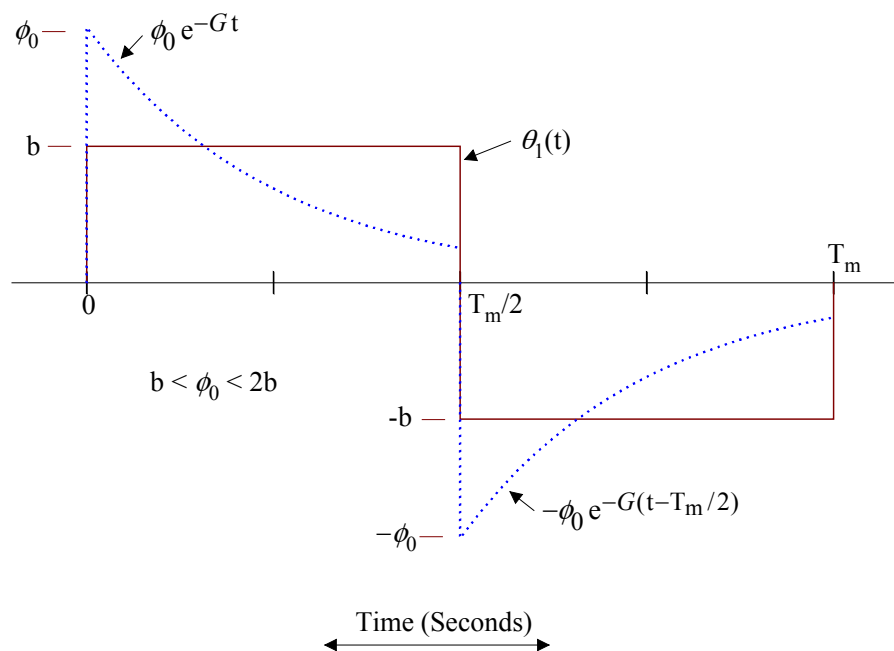

Fig. 3-15: One period of input θ_1 (solid-line plot), and one period of the steady-state closed loop phase error $\phi(t)$ (dashed-line plot). The phase error has discontinuous jumps of 2b every time input θ_1 jumps by 2b.

At $t = T_m/2$, $\phi(t)$ must drop from $\phi_0 \exp(-GT_m/2)$ to $\phi_0 \exp(-GT_m/2)$ - 2b. But, this last value must be exactly $-\phi_0$. Hence, we can write

$$\phi_0 \, e^{-GT_m/2} - 2b = -\phi_0 \tag{3-63}$$

and solve for

$$\phi_0 = \frac{2b}{1 + e^{-GT_m/2}} \, . \tag{3-64}$$

Note that ϕ_0 approaches 2b as T_m becomes large compared to time constant $1/G$; this observation should be obvious.

PLL as FM Demodulator

The PLL can be used to demodulate an FM signal. In the discussion of the linear model (see Figure 3-13), we saw that the VCO acts like an integrator. That is, VCO input voltage e(t) can be expressed as

$$e = K_v^{-1} \frac{d\theta_2}{dt} \, . \tag{3-65}$$

Now, if the loop is tracking the input FM signal

$$\sqrt{2} A \sin\left(\omega_i t + K_f \int^t m \right)$$

very well (all frequency components of m are well within the closed-loop bandwidth), we have $\theta_2 \approx \theta_1$ which is equivalent to

$$\theta_2 \approx \left(\omega_i t + K_f \int^t m \right) - \omega_0 t . \tag{3-66}$$

Hence, from (3-65), the VCO control voltage is

$$e \approx K_v^{-1} \left(\omega_\Delta + K_f m \right) . \tag{3-67}$$

So, message m(t) can be recovered from e(t), the loop filter output.

First-Order PLL With Constant Frequency Reference

    This PLL contains no loop filter (F(s) = 1), and its reference consists of a sinusoid at frequency ω_i. Set n = m = 0, $a_0 = b_0 = 1$ in (3-18) to obtain operators $L_1 = L_2 = 1$. Then use $\theta_1 = \omega_\Delta t$ in (3-28) to obtain

$$\frac{d\phi}{dt} = \omega_\Delta - G \sin \phi \tag{3-68}$$

as the equation that describes this first-order PLL. Loop detuning $\omega_\Delta \equiv \omega_i - \omega_0$ is assumed to be positive in what follows (if $\omega_\Delta < 0$, then replace ϕ by -ϕ to obtain the case $\omega_\Delta > 0$).

    The number of explicit constants in (3-68) can be reduced by utilizing $\tau \equiv G t$ to obtain

$$\frac{d\phi}{d\tau} = \omega_\Delta' - \sin \phi , \tag{3-69}$$

where $\omega_\Delta' \equiv \omega_\Delta / G > 0$. Since G is significantly larger than unity in practical applications, τ is referred to as the *slow-time variable*.

Phase Plane Analysis of a First-Order PLL

    Figure 3-16 depicts typical plots of $d\phi/d\tau$ versus ϕ for the first-order PLL; it represents graphically the differential equation given by (3-69). Plots of this type are referred to as *phase planes*, and they are useful in analyzing first and second-order nonlinear differential equations

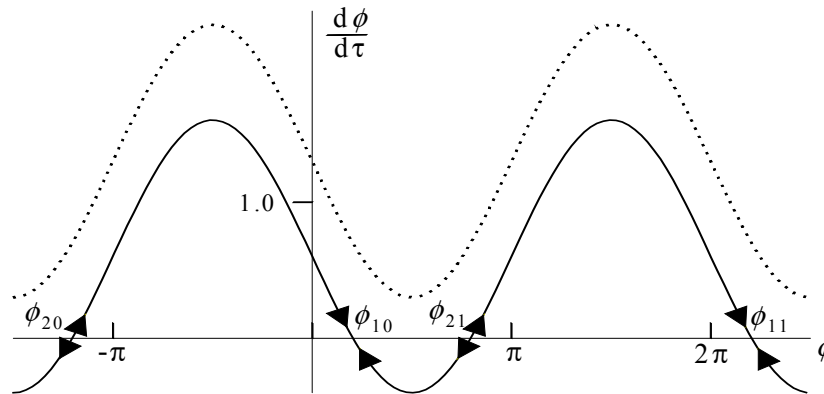**Figure 3-16:** Phase plane for a first-order PLL. Solid line graph depicts typical results for $0 < \omega_\Delta' < 1$. Dashed line plot depicts the case $\omega_\Delta' > 1$.

that have constant (*i.e.*, time-invariant) coefficients.

Phase Plane For the Case $0 \leq \omega_\Delta' < 1$

The solid-line plot on Fig. 3-16 was drawn to represent the case $0 \leq \omega_\Delta' < 1$. For ω_Δ' in this range, values of phase ϕ exist such that $d\phi/d\tau = 0$. These values of phase are known as *equilibrium points*. For (3-69), these points can be divided into two sets; the first is described by

$$\phi_{1k} = 2\pi k + \sin^{-1}\omega_\Delta', \tag{3-70}$$

and the second set is described by

$$\phi_{2k} = (2k-1)\pi - \sin^{-1}\omega_\Delta', \tag{3-71}$$

where k is an integer. At the points described by (3-70), the phase plane plot crosses the ϕ axis with a negative slope. The plot crosses the ϕ axis with a positive slope at the points described by (3-71).

The set of equilibrium points given by (3-70) represent stable phase-lock points of the first-order PLL. This follows from a simple argument that can be applied to point ϕ_{10} displayed on Fig. 3-16. First, assume that the phase error ϕ has a value which is slightly smaller than ϕ_{10} so that $d\phi/d\tau$ is positive. At this point, the phase error ϕ is increasing towards ϕ_{10}. Next, assume

that ϕ has a value slightly larger than ϕ_{10} so that $d\phi/d\tau$ is negative. At this point, ϕ is decreasing towards ϕ_{10}. Hence, the point ϕ_{10} is a stable phase-lock point of the PLL, and it follows that (3-70) describes the set of stable equilibrium points. In a similar manner, it is easy to argue that the equilibrium points described by (3-71) are unstable.

In general, the equilibrium points may vanish as ω_Δ increases through some positive value Ω_h. Now, a loop that is phase-locked becomes unlocked when its equilibrium points vanish. For this reason, Ω_h is known as the *hold-in range*, the value of ω_Δ at which the equilibrium points vanish. On Fig. 3-16, it is seen easily that the equilibrium points vanish for $\omega_\Delta' > 1$. For this reason, the hold-in range of the first-order PLL is $\Omega_h = G$.

Denoted here as Ω_p, the *pull-in range* of a first or second-order PLL with a constant frequency reference is the largest value of ω_Δ for which pull-in occurs regardless of initial conditions. If $|\omega_\Delta|$ is larger than Ω_p, there exists initial conditions from which the PLL can start and never pull-in successfully. From Fig. 3-16 and the discussion provided above, it is seen easily that the pull-in range of a first-order PLL is $\Omega_p = G$. Hence, a first-order PLL has identical pull-in and hold-in ranges.

Phase Plane For the Case $\omega_\Delta' > 1$

Consider the dotted-line plot on Fig. 3-16; this plot is typical of the case $|\omega_\Delta'| > 1$. Note that the value of (ϕ, $d\phi/d\tau$) never leaves this path. Also, the path does not intersect the ϕ axis; the system never makes it to an equilibrium point, so phase lock is not possible. In terms of quantities that can be observed in a first-order PLL, this path corresponds to a periodic beat note in the output of the phase comparator.

The period of this beat note can be computed. To accomplish this, solve (3-69) for

$$d\tau = \frac{d\phi}{\omega_\Delta' - \sin\phi} \,. \tag{3-72}$$

For the case $|\omega_\Delta'| > 1$, integrate the left-hand side of (3-72) from $\tau = 0$ to $\tau = T_p$ and the right-
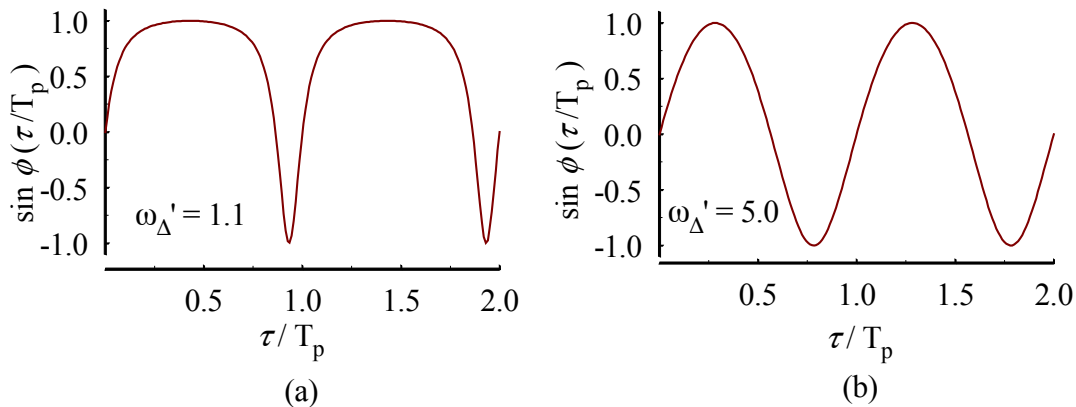
Figure 3-17: Normalized phase comparator output for a first-order PLL.

hand side from $\phi(0)$ to $\phi(T_p) = \phi(0) + 2\pi$ and write

$$
T_p = \int_0^{T_p} d\tau = \int_{\phi(0)}^{\phi(0)+2\pi} \frac{d\phi}{\omega_\Delta' - \sin\phi} .
\tag{3-73}
$$

The integral on the right-hand side of (3-73) can be found in most tables. From tabulated results, we obtain

$$
T_p = \frac{2\pi}{\sqrt{(\omega_\Delta')^2 - 1}} , \qquad \omega_\Delta' > 1 ,
\tag{3-74}
$$

as the period of the beat note. Note that T_p approaches infinity as ω_Δ' approaches unity from the right ($T_p \to \infty$ as $\omega_\Delta' \to 1^+$).

     For the case $|\omega_\Delta'| > 1$, a simple numerical computation yields the beat note in the phase comparator output. After starting from any initial condition, Equation (3-69) can be integrated numerically over one period, and this result can be used to calculate the beat note. Figures 3-17a and 3-17b depict typical plots of $\sin\phi(\tau/T_p)$ for $\omega_\Delta' = 1.1$ and $\omega_\Delta' = 5.0$, respectively. Both plots show two complete periods of the beat note. The nearly sinusoidal results depicted by Fig. 3-17b is characteristic of the large ω_Δ' case. However, as ω_Δ' decreases towards unity, the beat note becomes more unsymmetrical (so that it has a larger DC component)

as is shown by Fig. 3-17a.

Closed-Loop Transfer Function of First-Order PLL

Figure 3-13 with F $\equiv$ 1 illustrates the Laplace domain linear model of the first-order PLL. From (3-37), the closed-loop transfer function of this PLL is

$$H(s) = \frac{G}{s + G},$$ (3-75)

where G denotes a closed-loop gain factor. This result can be used with (3-39) to determine the VCO phase θ_2 for an arbitrary input θ_1. Coupled with (3-40), it can be used to determine the closed-loop phase error for an arbitrary input.

For $G > 0$, the pole of H(s) lies in the left half of the s-plane, and the first-order PLL is unconditionally stable. An inspection of (3-75) might lead to the naive and incorrect conclusion that phase lock is not possible for $G < 0$ since the pole of H would be in the right-half s-plane. However, the PLL with negative G has stable lock points that are displaced by π radians from the stable lock points that exist for positive G. Hence, without loss of generality, $G > 0$ can be assumed.

Transient and Steady-State Tracking Errors

The response of the first-order PLL is calculated easily for common inputs. Sample results are given below for the cases when the input reference is subjected to a phase step, frequency step, frequency ramp, and sinusoidal angle modulation. Of course, superposition applies for the linear model under consideration, so the results given below can be combined to produce more complicated input/output pairs.

As a first example, consider a reference subjected to a phase step. In this case, the reference is a sinusoid at frequency ω_0; the phase of this signal jumps by the constant θ_Δ so that

$$\theta_1(t) = \theta_\Delta \, U(t)$$

$$\Theta_1(s) = \frac{\theta_\Delta}{s} \, .$$

(3-76)

Along with (3-40), use this last result to obtain

$$\Phi(s) = [1 - H(s)]\Theta_1(s) = \frac{s}{s + G}\left[\frac{\theta_\Delta}{s}\right]$$

(3-77)

as the transform of the closed-loop phase error. Hence, the response of the first-order PLL to a phase step is simply

$$\phi(t) = \mathcal{L}^{-1}[\Phi(s)] = \theta_\Delta \, e^{-Gt} \, U(t) \, .$$

(3-78)

Finally, note that the steady-state response of the loop to a phase step is

$$\phi_{ss} = \lim_{t \to \infty} \phi(t) = 0 \, .$$

(3-79)

Consider applying a frequency step to the first-order PLL. In this case, at t = 0, the reference sinusoid jumps in frequency from ω_0 to ω_i. This implies an input phase given by

$$\theta_1(t) = \omega_\Delta t \, U(t),$$

(3-80)

where $\omega_\Delta \equiv \omega_i - \omega_0$ denotes the input frequency jump. In a manner similar to that used to obtain (3-78), the response of the PLL to this input is

$$\phi(t) = \frac{\omega_\Delta}{G}(1 - e^{-Gt}) \, .$$

(3-81)

Hence, the steady state error to a frequency step is

$$\phi_{ss} = \lim_{t \to \infty} \phi(t) = \frac{\omega_\Delta}{G} \, . \tag{3-82}$$

The first-order PLL incurs a constant steady-state phase error as the result of a frequency-stepped reference.

A first-order loop cannot track a frequency ramp. In this case, the relative phase of the signal is given in the time and Laplace domains as

$$\theta_1(t) = \frac{1}{2} R t^2 \, U(t) \tag{3-83}$$

and

$$\Theta_1(s) = \frac{R}{s^3} \, , \tag{3-84}$$

respectively, where R is a constant with units of radians/second^2. Due to the effects of Doppler, such a signal could be received from a constant frequency transmitter aboard a vehicle moving with a constant radial acceleration of Rc/ω_i meters/sec^2. Here, the quantity ω_i represents the frequency of the transmitted signal, and constant c denotes the speed of light in meters/second. The closed-loop phase error for this input is

$$\phi(t) = \frac{R}{G}(G t + e^{-G t} - 1) U(t) \, , \tag{3-85}$$

which was obtained by using techniques similar to those given by (3-78) and (3-81). Finally, note that this result is unbounded as t approaches infinity, so the first-order loop cannot track a

frequency-ramped reference.

As a last example of steady-state phase error calculation in a first-order PLL, consider the case involving an angle-modulated reference. Assume that a sinusoidal modulating signal is employed so that θ_1 has the form given by (3-51), where β is the modulation index, and ω_m is the frequency of the modulating signal. Now, use the transfer function given by (3-75) with the phase angle expression given by (3-58); the result of this combination is

$$\phi(t) = \frac{\omega_\Delta}{G} + \beta \left[\sin\omega_m t - \frac{G}{\sqrt{G^2 + \omega_m^2}} \sin(\omega_m t - \text{Tan}^{-1}(\omega_m / G)) \right]. \qquad (3-86)$$

This equation represents the steady-state tracking error in a first-order PLL with an angle modulated reference.

Consider the steady-state phase error given by (3-86) as a function of modulating frequency ω_m. Note that the sinusoidal portion of ϕ is small when $\omega_m \ll G$. In this case, the frequency of the external sinusoidal modulation is inside of the closed-loop bandwidth G, and the PLL tracks it with only a small error. However, the amplitude of the sinusoidal portion of ϕ is approximately β for $\omega_m \gg G$; in this case, the frequency of the external sinusoidal modulation is outside of the closed-loop bandwidth, and the PLL ignores it. Under these conditions, the PLL is locked to the carrier component of the reference, and it ignores the data sidebands.

The Second-Order PLL with a Perfect Integrator

Consider the second-order PLL with the loop filter

$$F(s) = 1 + \frac{\alpha}{s} . \qquad (3-87)$$

Note that the loop filter contains a perfect integrator. As discussed in this section, the PLL based on (3-87) has a number of important properties that make it a very attractive choice for many

applications.

        Loop filter (3-87) is implemented easily with modern operational amplifier technology. Figure 3-18 depicts a simple block diagram of such an implementation. Due to the virtual ground at the minus input of the operational amplifier, the input current is

$$i = v_1 / R_1.$$ (3-88)

But the input impedance of the OP-AMP is very high (ideally, infinite), so this current flows up through R_2 and C. Hence, output voltage v_2 is

$$v_2 = -R_2 i - \frac{1}{C} \int i \, .$$ (3-89)

Combine the last two equations to obtain

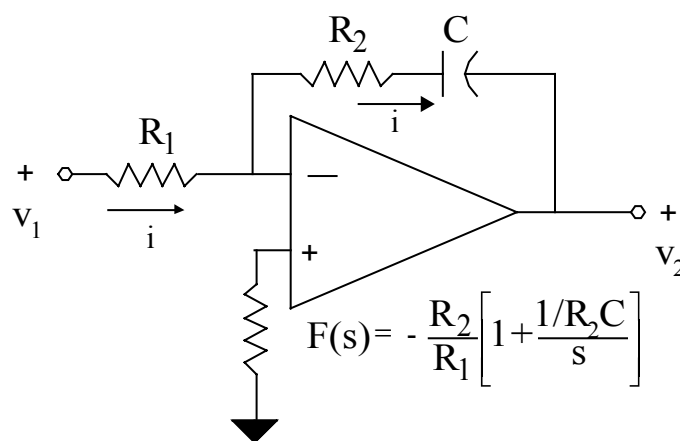$$v_2 = -R_2 i - \frac{1}{R_1 C} \int v_1 \, .$$ (3-90)

Fig. 3-18: Perfect integrator loop filter

In the Laplace domain, the loop filter transfer function can be written as

$$\frac{V_2(s)}{V_1(s)} = -\frac{R_2}{R_1}\left[1 + \frac{1/R_2C}{s}\right]. \tag{3-91}$$

In the closed-loop model, the constant R_2/R_1 in (3-91) enters into the closed loop gain constant G, and the minus sign only serves to shift the closed loop phase error by π (or $-\pi$ since $\sin(\phi \pm \pi)$ $= - \sin(\phi)$).

Transfer Function for Perfect Integrator Case

The linear, Laplace domain model of the PLL under consideration is depicted by Fig. 3-13 when loop filter F(s) is given by (3-87). For this model, the open loop transfer function is obtained easily; simply substitute (3-87) into (3-35) and write the open loop transfer function

$$G_0(s) = G\left[\frac{s+\alpha}{s^2}\right]. \tag{3-92}$$

Applying terminology from classical control theory, the PLL with open loop transfer function (3-92) is referred to as a *Type II* loop since $G_0(s)$ has two poles at the s-plane origin.

From (3-37), the closed-loop transfer function of the PLL is calculated easily as

$$H(s) = G\left[\frac{s+\alpha}{s^2 + Gs + \alpha G}\right], \tag{3-93}$$

which can be written in the commonly used form

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\zeta = \sqrt{G/4\alpha} \tag{3-94}$$

$$\omega_n = \sqrt{\alpha G} .$$

The quantities ζ and ω_n are the damping factor and natural frequency, respectively, of the PLL. Equation (3-93) can be used with (3-39) and (3-40) to determine the output phase and phase error for an arbitrary input.

Classical feedback control theory provides guidance in the selection of ζ and ω_n. In general, practical designs of this PLL strive to maintain $\zeta \approx 1/\sqrt{2}$ in order to achieve a fast step response (without ringing and excessive overshoot) for a given value of ω_n. Then, select ω_n large enough to meet specified settling-time requirements.

Loop Stability

The poles of (3-93) remain in the left-half s-plane for all $G > 0$; hence, this loop is unconditionally stable. This is best illustrated by the root locus plot depicted by Fig. 3-19. This diagram shows the locus of the closed-loop poles as gain G goes from zero to infinity. At $G = 0$, the poles break away from the real axis at s = 0; at $G = 4\alpha$, they return at the value s = -2α. For $G > 4\alpha$, the poles remain real valued; as $G \to \infty$, one pole approaches s = -α, and the other tends to minus infinity. This type of plot can be constructed easily using graphical techniques and the known location of the open-loop poles and zeros.

Transient and Steady-State Tracking Errors

The transient phase error response of the second-order Type II loop under consideration is calculated easily for common inputs. First, the phase error is calculated in the Laplace domain by using
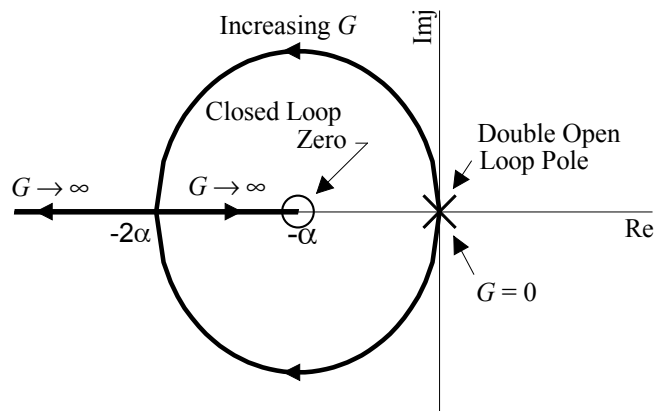
Figure 3-19: Root locus for a second-order PLL with a perfect integrator.

$$\Phi(s) = (1 - H(s))\Theta_1(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\Theta_1(s).$$ (3-95)

Then the desired results are obtained by taking the inverse Laplace transform of (3-95).

This method was used to produce the results provided in Table 1.1. The tabulated error responses were obtained for inputs consisting of the phase step described by (3-76), the frequency step described by (3-80), and the frequency ramp described by (3-83). As expected of the data in Table 1.1, the entries in the frequency step column are obtained by replacing θ_Δ by ω_Δ and integrating over $[0, t]$ the entries in the phase step column. A similar operation yields the frequency ramp column data from the frequency step column data.

Plots of these phase error functions are depicted by Figs. 3-20 through 3-22. Each figure contains a plot for the heavily over damped case ($\zeta = 2$) and the severely under damped case ($\zeta = .3$). Also, on each figure is a plot for $\zeta = 1/\sqrt{2}$, a highly desirable value of damping factor. For a fixed value of ζ, a plot similar to the ones depicted here can be used to determine a value for ω_n once the desired settling time is known.

	Phase Step (θ_Δ radians)	Frequency Step (ω_Δ rad/sec)	Frequency Ramp (R rad/sec^2)
$\zeta < 1$	$\theta_\Delta\left(\cos\sqrt{1-\zeta^2}\,\omega_n t - \dfrac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t \right)e^{-\zeta\omega_n t}$	$\left(\dfrac{(\omega_\Delta/\omega_n)}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t \right)e^{-\zeta\omega_n t}$	$\dfrac{R}{\omega_n^2} - \dfrac{R}{\omega_n^2}\left(\cos\sqrt{1-\zeta^2}\,\omega_n t + \dfrac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t \right)e^{-\zeta\omega_n t}$
$\zeta = 1$	$\theta_\Delta(1-\omega_n t)e^{-\omega_n t}$	$\dfrac{\omega_\Delta}{\omega_n}(\omega_n t)e^{-\omega_n t}$	$\dfrac{R}{\omega_n^2} - \dfrac{R}{\omega_n^2}(1+\omega_n t)e^{-\omega_n t}$
$\zeta > 1$	$\theta_\Delta\left(\cosh\sqrt{\zeta^2-1}\,\omega_n t - \dfrac{\zeta}{\sqrt{1-\zeta^2}}\sinh\sqrt{\zeta^2-1}\,\omega_n t \right)e^{-\zeta\omega_n t}$	$\left(\dfrac{(\omega_\Delta/\omega_n)}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t \right)e^{-\zeta\omega_n t}$	$\dfrac{R}{\omega_n^2} - \dfrac{R}{\omega_n^2}\left(\cosh\sqrt{\zeta^2-1}\,\omega_n t + \dfrac{\zeta}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t \right)e^{-\zeta\omega_n t}$

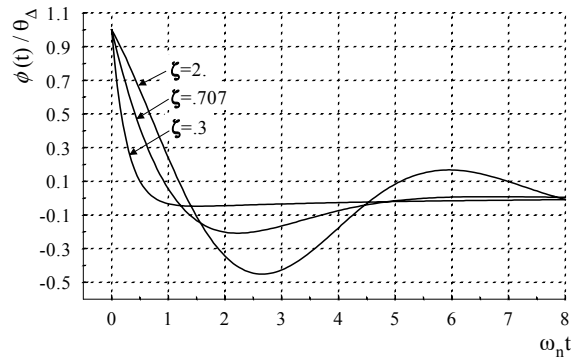**Table 1.1** Transient response of a second-order, Type II PLL containing a perfect integrator.

Figure 3-20: Normalized phase error due to a
phase step input.

The steady-state error response can be obtained from Table 1.1. Let $t \to \infty$ in these results to obtain respectively, where H is given by (3-94). Note the absence of a constant
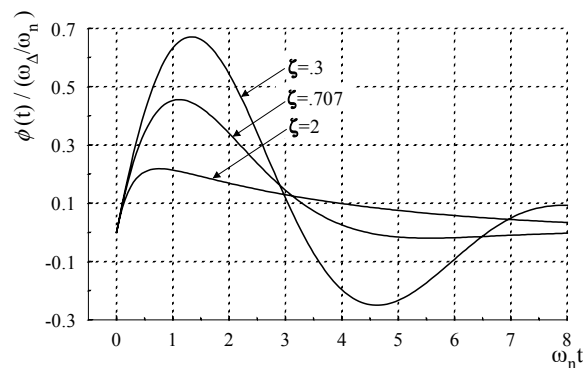
Figure 3-21: Normalized phase error due to a
frequency step input.

component in the phase error. This follows from the fact that this loop can track a frequency step with zero phase error.
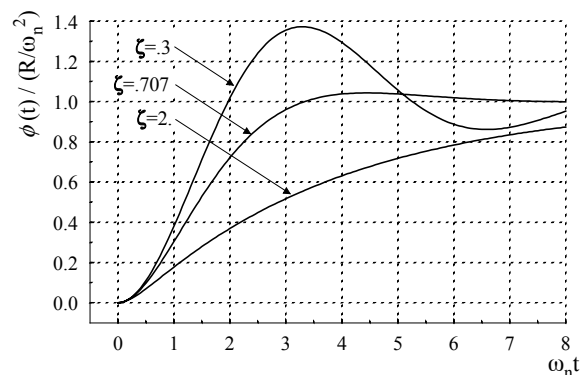
Figure 3-22: Normalized phase error due to a
frequency ramp input.

$$\phi_{SS} = \lim_{t \to \infty} \phi(t) = \begin{cases} 0 & \text{for a phase step} \\ 0 & \text{for a frequency step} \\ R / \omega_n^2 & \text{for a frequency ramp} \end{cases} \qquad (3\text{-}96)$$

for a second-order PLL with loop filter based on a perfect integrator.

It is interesting to compare (3-96) with similar results for the first-order PLL. This comparison points out some of the performance improvements which can be achieved by using a loop filter based on a perfect integrator. For example, the PLL that contains a perfect integrator in its loop filter out performs the first-order PLL when the reference is subjected to either a frequency step or a frequency ramp.

As a last example of steady-state tracking error in this second-order Type II PLL, consider the application of an angle modulated reference. Assume that angle θ_1 has the form given by (3-51), where β is the modulation index, and ω_m is the frequency of the modulating signal. In this case, the VCO steady-state relative phase and the steady-state phase error are

$$\theta_2(t) = \omega_\Delta t + \beta |H(j\omega_m)| \sin(\omega_m t + \angle H(j\omega_m)) \qquad (3\text{-}97)$$

$$\phi(t) = \beta \left[\sin \omega_m t - |H(j\omega_m)| \sin(\omega_m t + \angle H(j\omega_m)) \right], \qquad (3\text{-}98)$$

Figure 3-23 depicts frequency response plots of $|H(j\omega)|$ for several values of damping
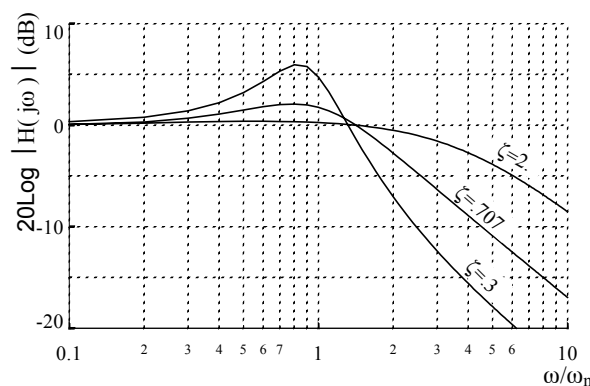

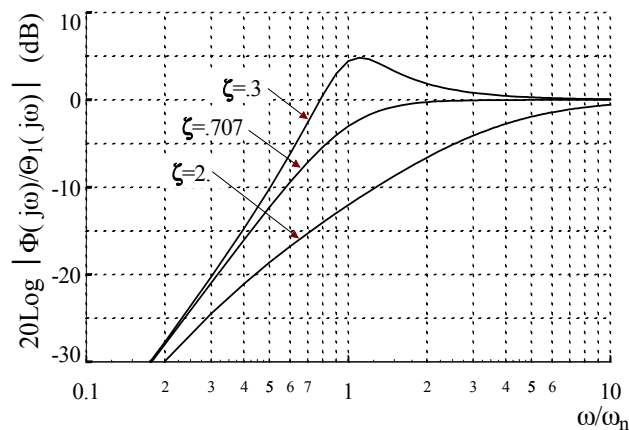**Figure 3-23:** Frequency response of a 2nd-order, Type II PLL.

Figure 3-24: Relative error.

factor ζ. This type of plot is useful for determining the magnitude of the sinusoidal component in θ_2. A similar type of plot for the relative error $|\Phi(j\omega)/\Theta_1(j\omega)|$ is given by Fig. 3-24. Note that the PLL tracks well the sinusoidal modulation as long as the frequency of this modulation is significantly less than the PLL natural frequency ω_n. However, the tracking error increases greatly as the modulation frequency approaches ω_n.

Phase Plane Analysis of Second-Order, Type II PLL

The PLL considered here has a loop filter given by (3-87). Also, it has a reference source that supplies a sinusoid at the constant frequency ω_i. This section contains a phase-plane analysis of this loop. It is shown that this loop can achieve phase lock for an arbitrary value of ω_i and for arbitrary initial conditions.

The equation that describes this loop can be obtained from (3-18) by setting $n = m = 1$, $a_1 = b_1 = 1$ and $a_0 = \alpha$ to obtain differential operators L_1 and L_2. Then, use L_1 and L_2 with (3-28) and $\theta_1 = (\omega_i - \omega_0)t = \omega_\Delta t$ to obtain

$$\frac{d}{dt}\left[\frac{d\phi}{dt} - \omega_\Delta\right] = -G\left[\frac{d}{dt} + \alpha\right]\sin\phi \tag{3-99}$$

$$\frac{d^2\phi}{dt^2} + G\cos\phi\frac{d\phi}{dt} + \alpha G\sin\phi = 0 \tag{3-100}$$

as the equation that describes the closed-loop phase error. Equation (3-100) is nonlinear and second-order; it is said to be autonomous, or time-invariant, since its coefficients α and G do not vary with time.

      The gain constant G in (3-100) can be eliminated by normalizing the time variable. This task is accomplished by using $\tau = Gt$ so that $d\phi/dt = G\,d\phi/d\tau$ and $d^2\phi/dt^2 = G^2\,d^2\phi/d\tau^2$. When τ is used as the independent variable, Equation (3-100) becomes

$$\frac{d^2\phi}{d\tau^2} + \cos\phi\,\frac{d\phi}{d\tau} + \alpha'\sin\phi = 0, \qquad\qquad (3\text{-}101)$$

where $\alpha' \equiv \alpha/G > 0$.

      Equation (3-101) can be represented by the first-order system

$$\frac{d\phi}{d\tau} = \dot\phi$$

$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad (3\text{-}102)$$

$$\frac{d\dot\phi}{d\tau} = -(\cos\phi)\dot\phi - \alpha'\sin\phi$$

in the dependent variables ϕ and $\dot\phi \equiv d\phi/d\tau$.

      The *equilibrium points* of (3-102) are defined as those constant values of ϕ, $\dot\phi$ that make the right-hand side of (3-102) vanish (i.e., $d\phi/d\tau = 0$ and $d\dot\phi/d\tau = 0$). All other points are called *ordinary points*. The equilibrium points of (3-102) are found by inspection to be

$$\phi = k\pi$$
$$\qquad\qquad , \qquad\qquad\qquad\qquad\qquad (3\text{-}103)$$
$$\dot\phi = 0$$

where k is an integer. By using perturbation techniques, it is easy to show that equilibrium points corresponding to even values of integer k are stable and those that correspond to odd k are

unstable (in the literature, the points for odd k are called *saddle points*).

The phase plane trajectories obey a first-order, ordinary differential equation. By simple division, it is possible to eliminate τ from (3-102) and obtain

$$\frac{d\dot{\phi}}{d\phi} = -\cos\phi - \alpha'\left[\frac{\sin\phi}{\dot{\phi}}\right] . \qquad (3\text{-}104)$$

This equation describes $\dot{\phi}$ as a function of ϕ. Note that the right-hand side of this equation is 2π-periodic in ϕ. This implies that ϕ can be taken modulo-2π; solutions of (3-104) may be restricted to the interval $-\pi \leq \phi < \pi$. Note that the right-hand side of (3-104) is indeterminate at the equilibrium points $(\phi, \dot{\phi}) = (k\pi, 0)$.

For the second-order PLL under consideration, plots of $\dot{\phi}$ versus ϕ are known as *phase plane plots*. Such plots can be made by numerically integrating (3-102) or (3-104). It can be shown that a unique solution of (3-102) passes through every ordinary point on the phase plane. Such a solution curve is referred to as a *trajectory* of the equation; the uniqueness property implies that two trajectories cannot cross each other.

Figure 3-25 depicts a phase plane plot for $\alpha' = 1$; for this value of integrator gain, the loop has $\zeta = 1/\sqrt{2}$, a desirable value of damping factor. Trajectories with $\dot{\phi} > 0$ move in the direction of increasing ϕ (upper-half plane trajectories move from left to right) while trajectories with $\dot{\phi} < 0$ move in the direction of decreasing ϕ (lower-half plane trajectories move from right to left). Also, when an upper-half plane trajectory reaches $\phi = \pi$, it is restarted at $\phi = -\pi$ with the same value of $\dot{\phi}$; likewise, lower-half plane trajectories that reach $\phi = -\pi$ are restarted at $\phi = \pi$. A *cycle slip* is said to have occurred every time ϕ changes by 2π. For every 2π increase in ϕ, the value of $\dot{\phi}$ decays by an amount that is small for large $\dot{\phi} > 0$, but the amount of decay increases with decreasing $\dot{\phi}$ (a similar statement can be made for lower-half plane trajectories) In a neighborhood of $(\phi, \dot{\phi}) = (0, 0)$, trajectories appear to spiral towards the origin.
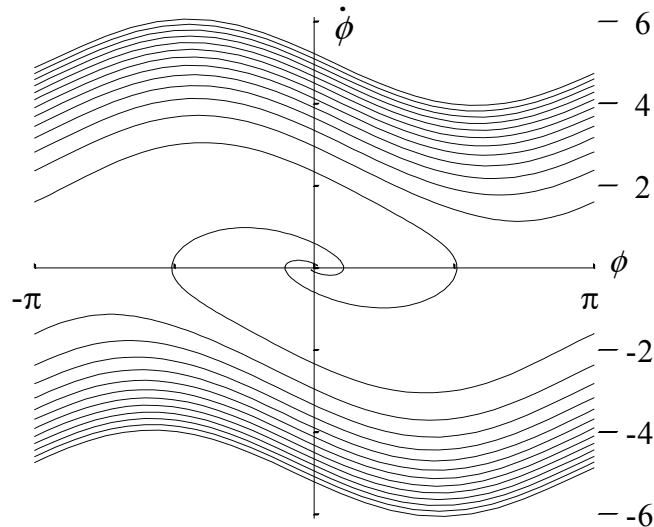
Figure 3-25: Phase plane plot for $\alpha' = 1$.

Other interesting elementary properties of these trajectories can be determined by inspection of (3-104). Trajectories that pass through ordinary points on the $\dot{\phi}$ axis do so with a slope of -1, while trajectories that pass through ordinary points on the ϕ axis do so with a slope of infinity. The phase plane plot is symmetrical; a trajectory remains a trajectory if both ϕ and $\dot{\phi}$ are negated. Finally, for very large $|\dot{\phi}|$, the first term dominates the second term on the right-hand side of (3-104), and the trajectories are nearly sinusoidal.

Pull In for a Second-Order Type II PLL

A process known as *pull in* is illustrated by Fig. 3-25. It is the phenomenon by which a PLL achieves phase lock naturally and without assistance. The second-order, Type II PLL has an infinite pull-in range. As shown in this section, phase lock occurs regardless of the value of ω_Δ and the initial conditions in effect when the loop is closed. Of course, these theoretical properties cannot be realized in applications; all practical PLLs have an upper limit on their pull-in range. In fact, the pull-in phenomenon is unreliable and slow in many practical applications. In these applications, additional circuits, that aid the acquisition process, are added to the PLL.

A simple argument leads to the fact that the PLL considered here has an infinite pull-in range. First, multiply both sides of (3-104) by $\dot{\phi}$ and integrate over $(-\pi, \pi)$ to obtain

$$\frac{1}{2}[\dot{\phi}^2(\pi) - \dot{\phi}^2(-\pi)] = -\int_{-\pi}^{\pi} \dot{\phi}\cos\phi\,d\phi - \alpha'\int_{-\pi}^{\pi}\sin\phi\,d\phi. \qquad (3\text{-}105)$$

The second integral on the right-hand side evaluates to zero, and the first can be evaluated by using integration by parts; these observations yield

$$\frac{1}{2}[\dot{\phi}^2(\pi) - \dot{\phi}^2(-\pi)] = \int_{-\pi}^{\pi} \sin\phi\,d\dot{\phi}. \qquad (3\text{-}106)$$

Now, Equation (3-104) can be used to produce

$$d\dot{\phi} = -(\cos\phi)\,d\phi - \alpha'\left[\frac{\sin(\phi)}{\dot{\phi}}\right]d\phi, \qquad (3\text{-}107)$$

and this result can be substituted into (3-106) to obtain

$$\frac{1}{2}[\dot{\phi}^2(\pi) - \dot{\phi}^2(-\pi)] = -\alpha'\int_{-\pi}^{\pi}\frac{\sin^2\phi}{\dot{\phi}}\,d\phi. \qquad (3\text{-}108)$$

Consider what Equation (3-108) implies about trajectories which lie in the upper-half of the phase plane. For these trajectories, the integrand $(\sin^2\phi)/\dot{\phi}$ is positive, and the right-hand side of (3-108) is negative. Hence, $\dot{\phi}$ decreases each time the PLL slips a cycle and the phase increases by 2π. In a similar manner, it is seen easily that trajectories in the lower-half plane experience an increase in $\dot{\phi}$ each time the PLL slips a cycle and the phase decreases by 2π. Therefore, regardless of initial conditions, $|\dot{\phi}|$ decreases each time the PLL slips a cycle; this fact implies an infinite pull-in range for the PLL under consideration.

The *pull-in time* is a function of the initial conditions, and it is defined as the time required for the PLL to go from this initial condition to a frequency-locked state. Roughly speaking, a frequency-locked state is reached when the PLL no longer slips cycles. The

nonlinear nature of the pull-in phenomenon prevents the determination of an exact formula for the pull-in time. However, for an initial value of $|\dot{\phi}| = \omega_\Delta' \equiv \omega_\Delta/G$, it can be shown that pull-in time grows proportional to the square of ω_Δ', for large ω_Δ' (i.e., when starting at $|\dot{\phi}| = \omega_\Delta'$ far from the origin of the phase plane, the pull-in process is "slow", and pull-in time is approximately proportional to the square of ω_Δ'). Hence, the fact that the second-order, Type II PLL has an infinite pull-in range is tempered by the observation that the time required to pull in grows at a rate that is proportional to the square of the initial frequency error when this value is large. In many applications, the pull-in phenomenon is too slow and unreliable. In these cases, the PLL contains additional circuitry specifically designed to aid the process of obtaining phase lock.

Costas Loop DSB Demodulator

Recall that a phase coherent carrier is required to demodulate a double sideband (DSB) modulated signal. At the receiver, the regeneration of such a carrier is made difficult by the fact that, in most applications, no carrier is transmitted (for efficiency reasons, the goal is to allocate all transmitter power to the data sidebands). In practice, this problem can be solved by using a *Costas loop* (invented by John P. Costas in the 1950's). A Costas loop can regenerate a phase-coherent carrier and demoduate DSB modulation at the same time. In digital communications, the Costas loop is used widely as a demodulator of binary phase shift key (BPSK) modulated (where $d(t) = \pm 1$ is a symmetrical binary data signal). The basic Costas loop can be modified (by including more channels) into a quadrature phase shift key (QPSK) demodulator. Such feedback-loop-based BPSK and QPSK demodulators are used in digital communication systems that must have a high degree of tolerance to noise (especially broadband Gaussian noise). Typical applications include wire-line data modems and deep-space digital communication systems.

On Fig. 3-26, the two *arm filters* are shown to have transfer function $H_a(s)$, and they are low pass in nature. In most application, simple RC filters are used so that $H_a(s) = 1/(1 + RCs)$; this arm-filter transfer function is used in the Costas loop model that is developed below. The
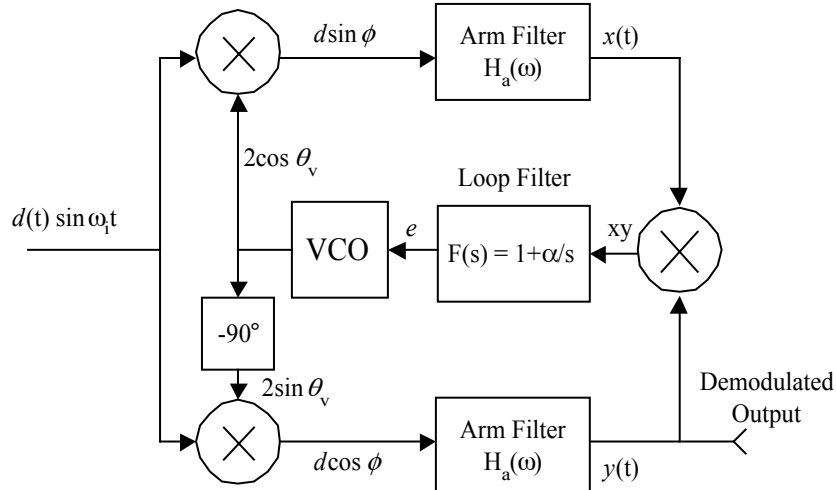
Fig. 3-26: Costas loop data demodulator. In most applications, the arm filters are simple RC low pass filters so that $H_a(s) = 1/(1+RCs)$.

arm filters must have sufficient bandwidth in order to pass the demodulated data without excessive distortion (usually, filter bandwidth is set at the data clock rate, or slightly higher).

A model is obtained easily for the Costas loop depicted by Fig. 3-26. Assuming first-order RC arm filters with $\omega_0 \equiv 1/RC$ (this is the RC filter cut-off frequency in radians/second), we can write

$$\frac{dx}{dt} = -\omega_0 x + \omega_0 d \sin \phi$$

$$\frac{dy}{dt} = -\omega_0 y + \omega_0 d \cos \phi$$
(3-109)

The loop filter dynamics are modeled by the first-order differential equation

$$\frac{d}{dt} e = \alpha xy + \frac{d}{dt} xy = \alpha xy + y\left[-\omega_0 x + \omega_0 d \sin \phi\right] + x\left[-\omega_0 y + \omega_0 d \cos \phi\right]$$

$$= \left[\alpha - 2\omega_0\right] xy + \omega_0 d \left[x \cos \phi + y \sin \phi\right].$$
(3-110)

The VCO is modeled (as always) by $d\theta_v/dt = \omega_0 + K_v e$, where ω_0 and K_v are the VCO center

frequency and gain, respectively. This VCO model leads to

$$\frac{d}{dt}\phi = \omega_\Delta - K_v e, \tag{3-111}$$

where $\phi \equiv \omega_i t - \theta_v$ is the closed-loop phase error, and $\omega_\Delta \equiv \omega_i - \omega_0$ is the loop de-tuning parameter. Equations (3-109) through (3-111) model the Costas loop, and the independent (state) variables x, y, e and ϕ describe the Costas loop.

When phase-locked and operating properly, the closed-loop phase error $\phi = 0$. With this value of ϕ, we obtain $e = \omega_\Delta/K_v$ from (3-111). With $\phi = 0$, we observe that $x = 0$ and y satisfies

$$\frac{dy}{dt} = -\omega_0 y + \omega_0 d, \tag{3-112}$$

an equation that describes an RC low pass filter driven by data signal d. Finally, $y \approx d$ if the bandwidth ω_0 of the arm filters is sufficient to prevent significant amplitude and phase distortion in the demodulated data, and we have demodulated the digital data.

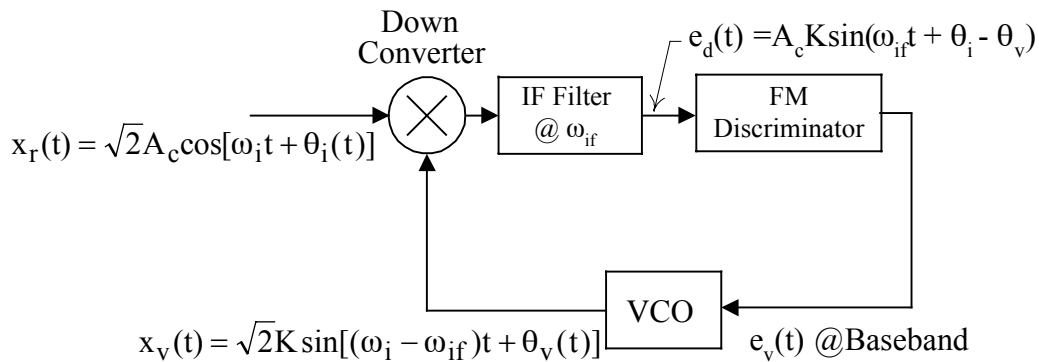**FM Demodulation Using Frequency-Compressive Feedback**

Consider the FM demodulator depicted by Figure 3-27. The input to the demodulator is

$$x_r(t) = \sqrt{2}A_c \cos[\omega_i t + \theta_i(t)], \tag{3-113}$$

an angle-modulated signal. The VCO output is

$$x_v(t) = \sqrt{2}K \sin[(\omega_i - \omega_{if})t + \theta_v(t)], \tag{3-114}$$

where $\omega_i - \omega_{if}$ is the VCO's center frequency (the VCO gain is Kv). Hence, we have

FM Discriminator: Center Freq $= \omega_{if}$, Gain $= K_d$

VCO: Center Freq $= \omega_i - \omega_{if}$, Gain $= K_v$

Figure 3-27: Frequency feedback demodulator.

$$\frac{d\theta_v}{dt} = K_v e_v \tag{3-115}$$

as the VCO equation.

The output of the down converter contains both sum and difference frequency terms. The difference frequency term is at ω_{if}, the center frequency of the IF filter and discriminator. Assume that the difference frequency term is passed without amplitude or phase distortion by the IF filter. The sum frequency term falls outside of the IF filter, and it can be ignored. Hence, the output of the IF filter can be written as

$$e_d(t) = A_c K \sin[\omega_{if} t + \theta_i(t) - \theta_v(t)]. \tag{3-116}$$

Also, this is the input to the discriminator.

The center frequency of the discriminator is ω_{if}. Hence, the base band discriminator output is

$$e_v(t) = \frac{1}{2\pi} K_d \frac{d}{dt}[\theta_i(t) - \theta_v(t)] = \frac{1}{2\pi} K_d \left[\frac{d\theta_i(t)}{dt} - K_v e_v \right]. \tag{3-117}$$

This last equation can be solved for

$$\left[1 + \frac{K_d K_v}{2\pi}\right] e_v = \frac{1}{2\pi} K_d \frac{d\theta_i(t)}{dt} \;\Rightarrow\; e_v = \left[\frac{K_d / 2\pi}{1 + K_d K_v / 2\pi}\right] \frac{d\theta_i(t)}{dt}, \tag{3-118}$$

which shows that base band e_v is proportional to the input frequency deviation, and we have an FM demodulator.

Assume that the input signal is FM modulated so that

$$\theta_i(t) = 2\pi f_d \int^t m, \tag{3-119}$$

where m(t) is a message. Use (3-118) and (3-119) to write

$$e_v(t) = \left[\frac{K_d f_d}{1 + K_d K_v / 2\pi}\right] m(t), \tag{3-120}$$

so that we have demodulated the input and recovered the message.

This type of FM demodulator has certain advantages over a straight FM discriminator for the case of wide band FM (where the deviation ratio D is large so that the transmission bandwidth is large compared to the message bandwidth). The advantage of this technique (over a straight discriminator) is seen by examining (3-116), the discriminator input. In (3-116), we can use (3-115) and (3-118) to write

$$\theta_i(t) - \theta_v(t) = \theta_i(t) - K_v \int^t e_v = \theta_i(t) - K_v \left[\frac{K_d / 2\pi}{1 + K_d K_v / 2\pi}\right] \theta_i(t)$$

$$= \left[\frac{1}{1 + K_d K_v / 2\pi}\right] \theta_i(t). \tag{3-121}$$

Hence, the discriminator's input can be written as

$$
\begin{aligned}
e_d &= A_c K \sin\left[\omega_{if} t + \left\{ \frac{1}{1 + K_d K_v / 2\pi} \right\} \theta_i(t) \right] \\
&= A_c K \sin\left[\omega_{if} t + 2\pi \left\{ \frac{f_d}{1 + K_d K_v / 2\pi} \right\} \int^t m(\tau) d\tau \right]
\end{aligned}
\tag{3-122}
$$

As supplied to the ideal FM discriminator, the FM signal e_d has a modulation index of $f_d/[1 + K_d K_v/2\pi]$ Hz/volt. By making $K_d K_v \gg 2\pi$, a significant reduction can be effected in the modulation index and frequency deviation of the discriminator input signal. The effective deviation ratio D, as seen by the discriminator, can be reduced significantly. Equivalently, the bandwidth of the discriminator input can be reduced (a wide band FM signal on the demodulator's input shows up as a narrow band FM signal on the discriminator input). The input wideband FM signal has been "compressed" into a narrow band FM signal.

Why is this significant? Well, it turns out that FM demodulation is subjected to a *threshold phenomenon*. Basically, things "work well" if the input signal-to-noise ratio is above threshold. But, performance (SNR in the demodulator output) degrades sharply when input signal-to-noise ratio falls below threshold. By "compressing" the signal and reducing the equivalent bandwidth seen by the discriminator (so that a narrow IF filter can be used), it is possible to reduce the noise power seen by the discriminator, and this will result in a reduced FM threshold. For example, on commercial wide band FM (where D = 75/15 = 5), it is possible to reduce the threshold by around four-to-five dB, according to published reports.