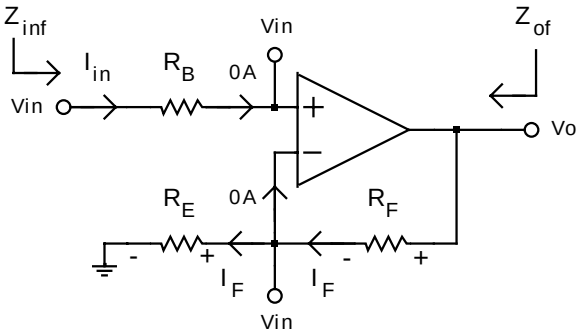
BASIC OPERATIONAL AMPLIFIER CIRCUITS

1. NON-INVERTING AMPLIFIER

$$A_{VF\ (ideal)} = \frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_E}$$

$$Z_{IF\ (ideal)} = \frac{V_{in}}{I_{in}} = \infty$$

$$Z_{OF\ (ideal)} = \frac{V_o}{I_o}\bigg|_{V_{in}=0} = 0$$



For minimum O/P DC offset voltage, make $R_B \approx R_E \| R_F$ with BJT input op amps.

For FET input op amps, in general, omit R_B. If R_E and R_F are very large (MΩ), do use $R_B \approx R_E \| R_F$. to minimise O/P DC offset voltage.

NOTE: The ideal gain is positive therefore the output is in phase with the input which explains why this circuit is called a non-inverting amplifier. This circuit is also ideal for buffering purposes, that is to isolate the load from the source since $Z_{IF} = \infty$ and $Z_{OF} = 0$ - the source does not supply any current ($I_{in} = 0$) while the load current is supplied by the output of the op amp which has 0Ω ideal output impedance.

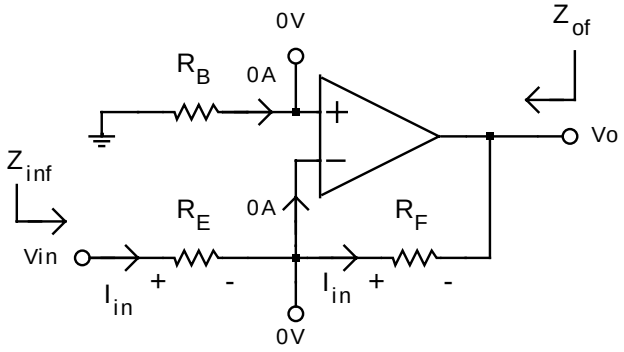
Derivation of A_{VF} and Z_{IF} ideal

2. INVERTING AMPLIFIER

$$A_{VF\ (ideal)} = \frac{V_o}{V_{in}} = -\frac{R_F}{R_E}$$

$$Z_{IF\ (ideal)} = \frac{V_{in}}{I_{in}} = R_E$$

$$Z_{OF\ (ideal)} = \left.\frac{V_o}{I_o}\right|_{V_{iu}=0} = 0$$



For minimum O/P DC offset voltage, make $R_B \approx R_E \| R_F$ with BJT input op amps.

For FET input op amps, in general, omit R_B. If R_E and R_F are very large (MΩ), do use $R_B \approx R_E \| R_F$. to minimise O/P DC offset voltage.

NOTE: The gain is negative therefore the output is inverted with respect to the input. The input impedance is not infinite therefore current is drawn from the source - this is not a buffer as seen with the non-inverting amplifier.

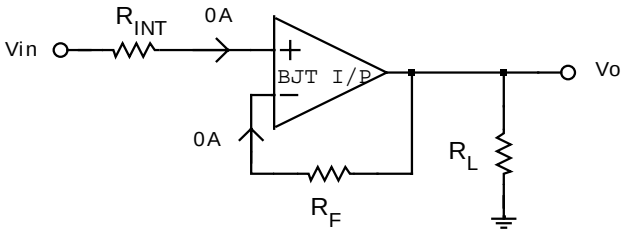
Derivation of A_{VF} and Z_{IF} ideal

3. UNITY-GAIN BUFFER

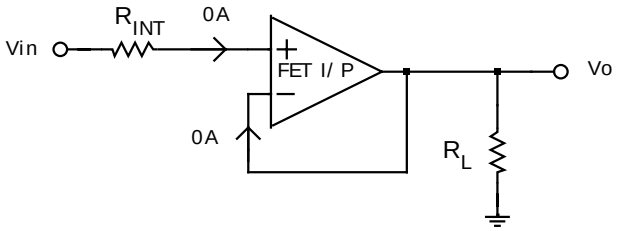
$$A_{VF\ (ideal)} = \frac{V_o}{V_{in}} = 1$$

$$Z_{IF\ (ideal)} = \frac{V_{in}}{I_{in}} = \infty$$

$$Z_{OF\ (ideal)} = \left.\frac{V_o}{I_o}\right|_{V_{iu}=0} = 0$$



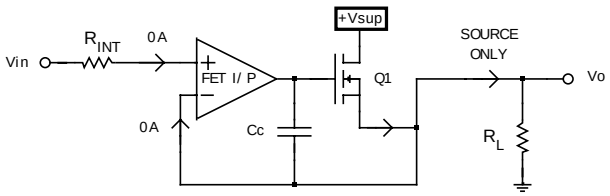
For minimum O/P DC offset voltage, make $R_F \approx R_{INT}$ with BJT input op amps.



For FET input op amps, in general, omit R_F If R_{INT} is very large (MΩ), do use $R_F \approx R_{INT}$. to minimise O/P DC offset voltage.

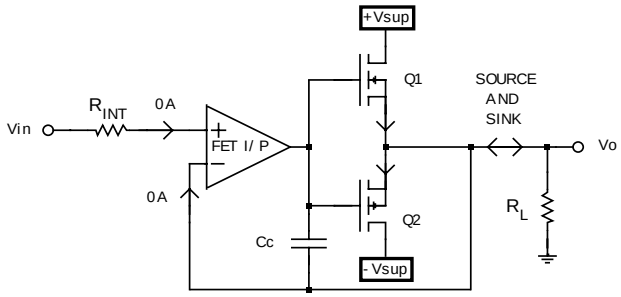
NOTE: This circuit is ideal for buffering purposes, that is to isolate the load from the source since $Z_{IF} = \infty$ and $Z_{OF} = 0$ - the source does not supply any current ($I_{in} = 0$) while the load current is supplied by the output of the op amp which has 0Ω output impedance.

Current boosting-source only



C_C = 20 pF to 0,1 µF needed to stabilise the feedback loop - the larger the input stray capacitance of the MOSFET is, the larger C_C must be. Larger C_C values yield smaller bandwidth and smaller slew rate (dV_o/dt max). If C_C is too small, the feedback loop may break into self oscillations - unstable feedback loop.

Current boosting-source and sink (push-pull output)



Derivation of A_{VF} and Z_{IF} ideal

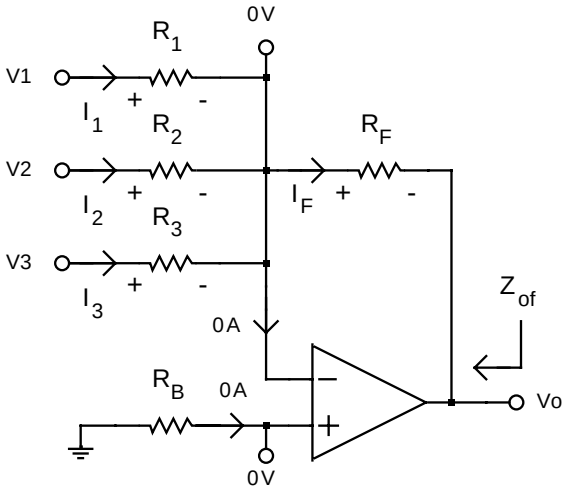
4. SUMMING AMPLIFIER (inverting)

$$V_o = -\left[\left(\frac{R_F}{R_1}\times V_1\right)+\left(\frac{R_F}{R_2}\times V_2\right)+\left(\frac{R_F}{R_3}\times V_3\right)\right]$$

$$If \;\; R_1 = R_2 = R_3 = R_E \quad \Rightarrow \quad V_o = -\frac{R_F}{R_E}\left[V_1 + V_2 + V_3\right]$$

$$Z_{IF1} = \frac{V_1}{I_1} = R_1 \qquad Z_{IF2} = \frac{V_2}{I_2} = R_2 \qquad Z_{IF3} = \frac{V_3}{I_3} = R_3$$

$$Z_{OF} = \left.\frac{V_o}{I_o}\right|_{V_{in}=0} = 0$$

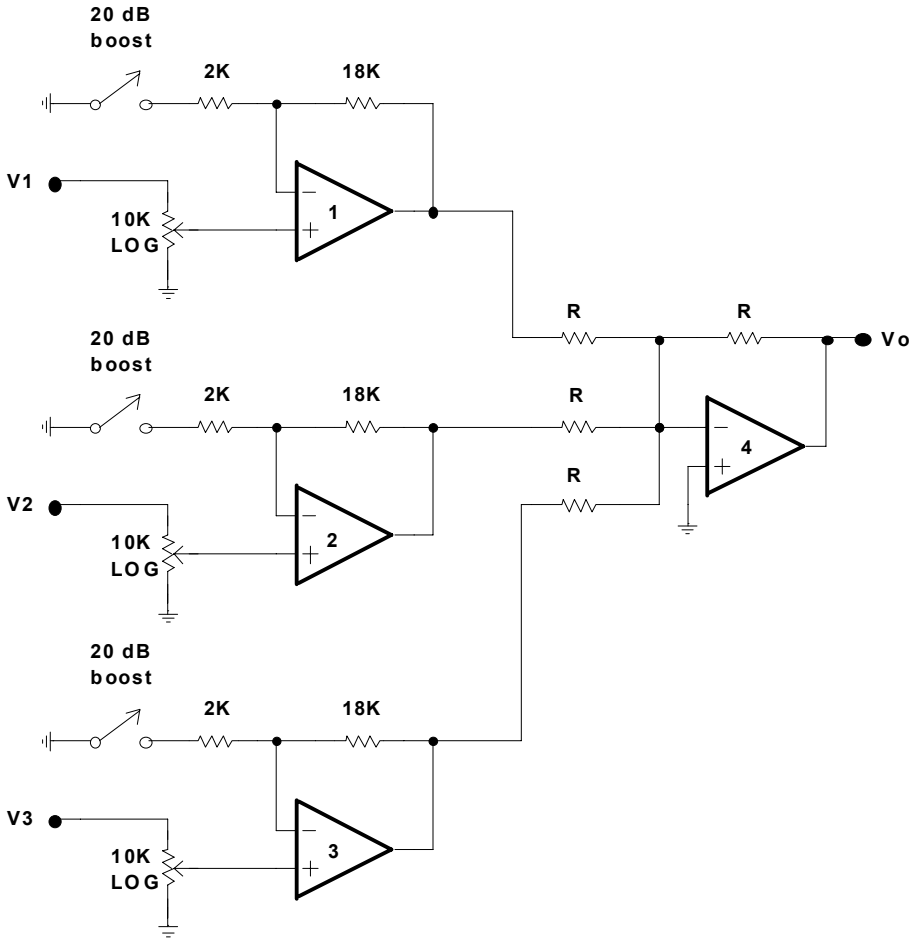


For minimum O/P DC offset voltage, make $R_B \approx R_1 \| R_2 \| R_3 \| R_F$ with BJT input op amps.

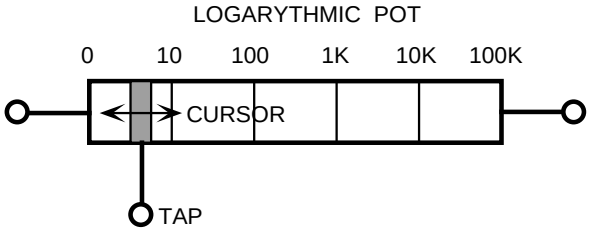
For FET input op amps, in general, omit R_B. If resistors are very large (MΩ), do use $R_B \approx R_1 \| R_2 \| R_3 \| R_F$. to minimise O/P DC offset voltage.

Derivation of A_{VF} and Z_{IF} ideal

5. AUDIO MIXER



NOTE: Audio volume control pots should vary logarythmically because the human ear responds logarythmically to the amplitude of the signal. This means that if we use a slide pot, as we slide the cursor in a linear fashion, the resistance increases logarythmically which results in a linear increase of the sound volume perceived by the human ear.

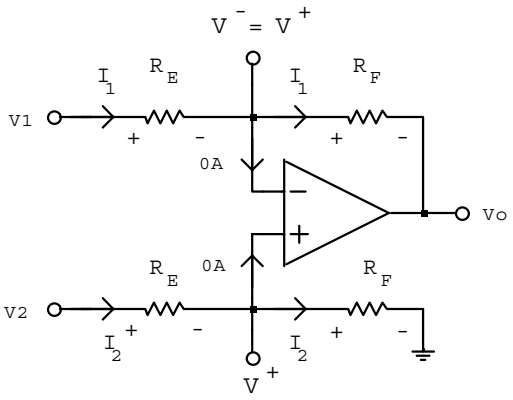


6. SUBTRACTOR #1 (matched resistors)

$$V_o = \frac{R_F}{R_E}[V_2 - V_1]Z_{OF} = \left.\frac{V_o}{I_o}\right|_{V_{iu}=0} = 0$$

$$Z_{IF1(\text{var}\,iable)} = \frac{V_1}{I_1} = \frac{R_E}{1-\left(\frac{R_F}{R_E+R_F}\frac{V_2}{V_1}\right)}$$

$$Z_{IF2\,(fixed)} = \frac{V_2}{I_2} = R_E + R_F$$



Both op amp inputs see $R_E \| R_F$ resistance wise therefore DC O/P offset is minimised.

Derivation of A_{VF} and Z_{IF} ideal

6. SUBTRACTOR #1 (unmatched resistors)

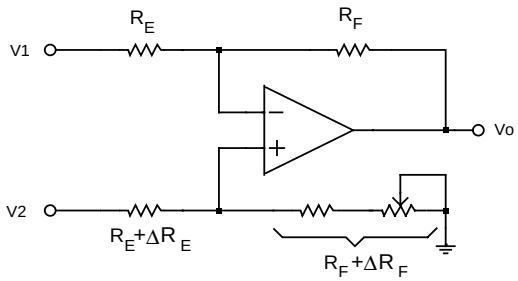
$$A_d = \frac{V_o}{V_2 - V_1} = \frac{R_F}{R_E}\left[0{,}5 + \frac{0{,}5\left(1 + \left(\Delta R_F / R_F\right)\right)}{1 + \left(\frac{\Delta R_E + \Delta R_F}{R_E + R_F}\right)}\right] \approx \frac{R_F}{R_E}$$

$$A_{cm} = \frac{V_o}{V_{in}} = \frac{R_F}{R_E + R_F}\left[\frac{\frac{\Delta R_F}{R_F} - \frac{\Delta R_E}{R_E}}{1 + \frac{\Delta R_E + \Delta R_F}{R_E + R_F}}\right]$$

$$\frac{1}{CMRR_{TOT}} = \left(1 + \frac{R_F}{R_E}\right)^{-1} \times \left[\frac{\frac{\Delta R_F}{R_F} - \frac{\Delta R_E}{R_E}}{1 + \frac{\Delta R_E + \Delta R_F}{R_E + R_F}}\right]^{-1} + \frac{1}{CMRR_{OPA}}$$

$$\frac{1}{CMRR_{TOT}}\min = \left(1 + \frac{R_F}{R_E}\right)^{-1} \times \left(2TOL_R\right) + \frac{1}{CMRR_{OPA}}$$

$$V_o = A_d\left(V_2 - V_1\right) + A_{cm}\left(\frac{V_1 + V_2}{2}\right)$$



Both op amp inputs see $R_E \| R_F$ resistance wise therefore DC O/P offset is minimised.

A_{CM} is the voltage gain when common inputs are used, that is $V_{in} = V_1 = V_2$.

Component mismatch usually determines A_{CM} of the subtractor when discrete resistors are used and one should use a trim pot to null A_{CM} - with both inputs tied together, apply a large AC input and measure the AC output on a sensitive scale while trimming the pot until the output reaches zero mV AC or reaches a minimum level. Even with optimal setting of the pot, A_{CM} cannot be exactly zero because of the op amp's own A_{CM} which has nothing to do with the external resistor mismatch. So the story is that even with perfectly matched components, there will always be a residual A_{CM} .

One can purchase a subtractor with all the resistors integrated and matched right on the chip for a good CMRR. If the CMRR is not satisfactory, there is usually provisions for external trimming of A_{CM}.

CMRR VALUES for $A_d = R_F/R_E$ = 10 V/V and $CMRR_{OPA}$ = 100 dB					
% TOLERANCE	10	1	0,1	0,01	0,001
$CMRR_{ideal}$	34,8 dB	54,8 dB	74,8 dB	94,8 dB	114,8 dB
$CMRR_{actual}$	34,8 dB	54,76 dB	74,3 dB	91 dB	98,55 dB

$CMRR_{ideal}$ is with an ideal op amp whose A_{cm} = 0 V/V and $CMRR_{actual}$ is for an actual op amp with $A_{cm}=A_d/100K$.

7. SUBTRACTOR #2 (high voltage)

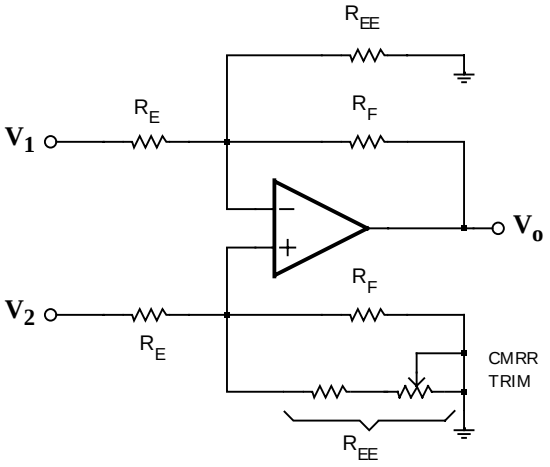
$$A_d = \frac{V_o}{V_2 - V_1} = \frac{R_F}{R_E}$$

$$A_{cm} = \frac{V_o}{V_{in}} \quad for \quad V_{in} = V_1 = V_2$$

$$V_o = A_d(V_2 - V_1) + A_{cm}\left(\frac{V_1 + V_2}{2}\right)$$

Both op amp inputs see $R_E \| R_{EE} \| R_F$ resistance wise therefore DC O/P offset is minimised.

R_{EE} does not affect the differential gain A_d but attenuates the input voltages to a low value that can be handled by the op amp inputs. For instance, V1 and V2 can be above 100V but R_{EE} can be selected such that $V^+ = V^- < V_{in}$ max of op amp - V_{in} max is usually a few volts below and above the positive and negative supply voltages respectively.



The pot is used to maximise the CMRR in spite of component mismatch.

8. SUBTRACTOR #3 (high input impedance)

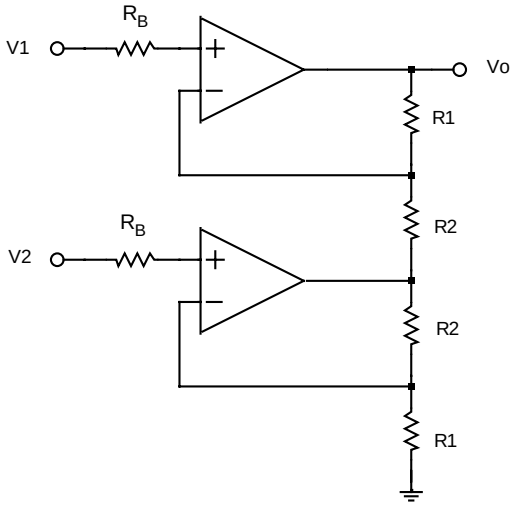
$$A_d = \frac{V_o}{V_1 - V_2} = 1 + \frac{R_1}{R_2}$$

$$A_{cm} = \frac{V_o}{V_{in}} \quad for \quad V_{in} = V_1 = V_2$$

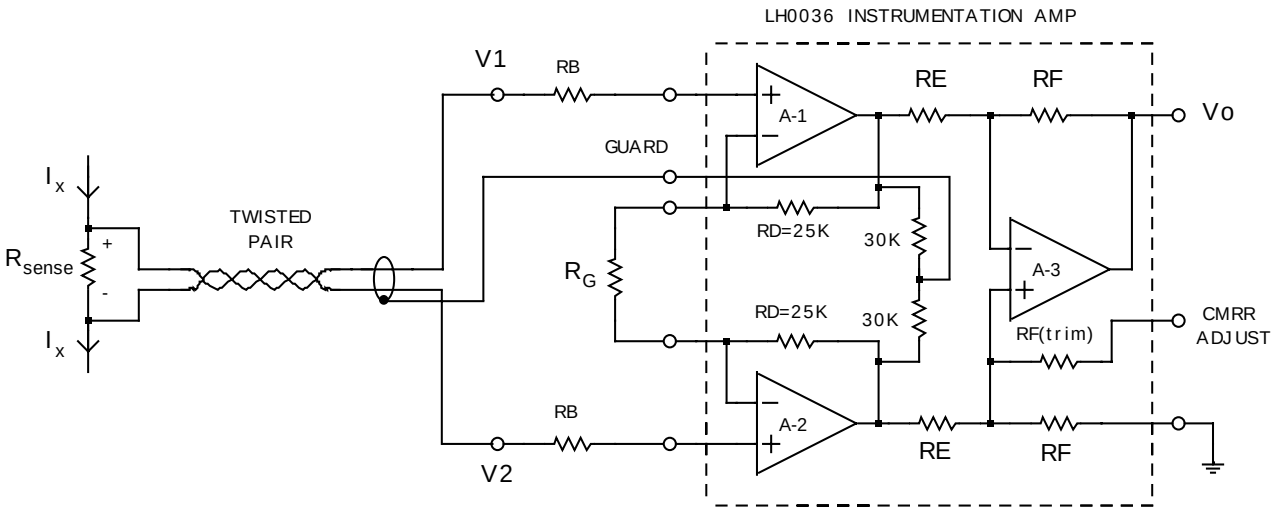
$$V_o = A_d(V_1 - V_2) + A_{cm}\left(\frac{V_1 + V_2}{2}\right)$$

$R_B = R_1 \| R_2$ for minimum DC O/P offset.

Resistors are not perfectly matched, therefore one of the resistors should be trimmed to obtain maximum CMRR (or minimum A_{CM}).



9. INSTRUMENTATION AMPLIFIER (high input impedance)



$$A_d = \frac{V_o}{V_2 - V_1} = 1 + \frac{2R_D}{R_G} = 1 + \frac{50K}{R_G}$$

$$A_{cm} = \frac{V_o}{V_{in}} \quad for \quad V_{in} = V_1 = V_2$$

$$V_o = A_d(V_2 - V_1) + A_{cm}\left(\frac{V_1 + V_2}{2}\right)$$

$R_B = R_D \| (R_G + R_D)$ for minimum DC O/P offset.

CMRR adjustment

Resistors R_E and R_F are equal therefore the second stage is a unity-gain subtractor. The resistors integrated on the chip are not perfectly matched which yields different values of CMRR depending on the differential gain being used - see data sheets. For better CMRR values, one can connect a 5K pot from the "CMRR ADJUST" pin to ground for trimming purposes - if not used, the pin must be floated.

Input guarding: a guard drive pin with a 15K resistance is provided. This pin will drive the guard at the common mode input voltage (that is at $(V_1+V_2)/2$) to minimise leakage currents picked up by the normal inputs - the leakage currents are then picked up by the guard. In some applications the guard should be driven with 0Ω impedance with a unity-gain buffer whose input is connected to the guard pin of the LH0036.

Twisted pair: if remote sensing is done the wires carrying the signal will pick up stray AC signals (magnetic induction). If the wires are twisted they will pick up about the same amount of signal which will appear as a common mode input and will be heavily attenuated by the instrumentation amplifier if it has a good CMMR.

Shielding: In very noisy (electrical noise) environments, the twisted pair should be shielded to prevent any pick up from outside.

In the above circuit shown, the voltage across R_{sense} is sensed remotely and is amplified by the instrumentation ampifier.

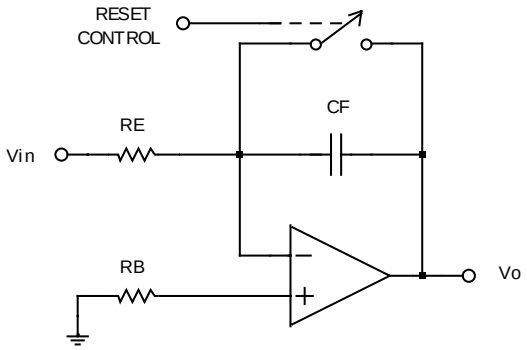
$$V_o = A_d \times (V_2 - V_1) = \left[1 + \frac{50K}{R_G}\right] \times I_X R_{sense} \qquad \text{assuming } A_{CM} = 0$$

9. IDEAL INVERTING INTEGRATOR

$$V_{o(t_2)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(t)}\,dt + V_{o(t_1)}$$

$$Z_{IF\ (ideal)} = \frac{V_{in}}{I_{in}} = R_E$$

$$Z_{OF\ (ideal)} = \left.\frac{V_o}{I_o}\right|_{V_{iu}=0} = 0$$



$R_B = R_E$ for minimum O/P DC offset.

Derivation of $V_o(t)$

$$I_{in} = V_{in} / R_E \qquad V_o = -V_C \qquad I_C = I_{in} = C_F \frac{dV_C}{dt} \quad \Rightarrow \quad dV_C = \frac{I_{in}}{C_F}dt \quad \Rightarrow \quad V_C = \int \frac{I_{in}}{C_F}dt + K$$

where K is the integration constant.

$$V_o = -V_C = -\int \frac{I_{in}}{C_F}dt - K = -\int \frac{V_{in}}{R_E C_F}dt - K = -\frac{1}{R_E C_F}\int V_{in}dt + K' \quad where \quad K' = -K$$

$$V_{o(t_2)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(t)}\,dt + K'$$

Now to find the integration constant, let $t_2 \to t_1$ and let us solve the following limit:

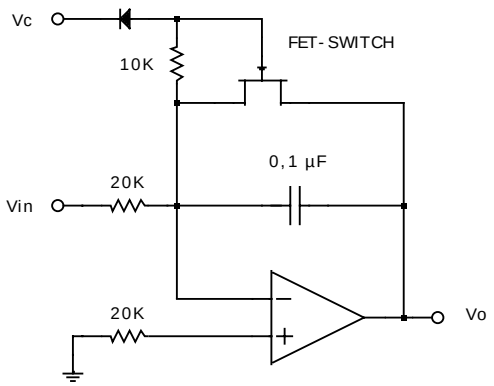
$$\underset{t_2 \to t_1}{Lim}\left(V_{o(t_2)}\right) = V_{o(t_1)} = \underset{t_2 \to t_1}{Lim}\left(-\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(t)}\,dt + K'\right) = K' \qquad \text{therefore } K' = V_o\,(t_1)$$

The integral is zero as $t_2 \to t_1$ and the O/P is given by $V_{o(t_2)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(t)}\,dt + V_{o(t_1)}$

When using the above formula to determine the output, $V_o(t_1)$ will always be V_o at the start of the integration period and $V_o(t_2)$ will be V_o at end of the integration period.

Reset control

At the end of the integration period the output can be reset to zero by discharging the capacitor and keeping it discharged by leaving the switch ON (closed). If the switch is left OFF (open), even if there is no input signal, the capacitor will be slowly charged by a very small DC leakage current caused by the small DC input offset voltage of the op amp (V_{io}) and the small input bias currents of the op amp which would cause the capacitor to charge until saturation of the output is reached. The switch should be open only during the integration period when the capacitor is being charged by the input current which is normally much larger than the DC leakage current.



Example: Integration of an aperiodic waveform

Determine the output waveform given the input waveform shown below assuming that the capacitor is initially discharged, that is the FET switch is turned OFF only at the start of the integration period.

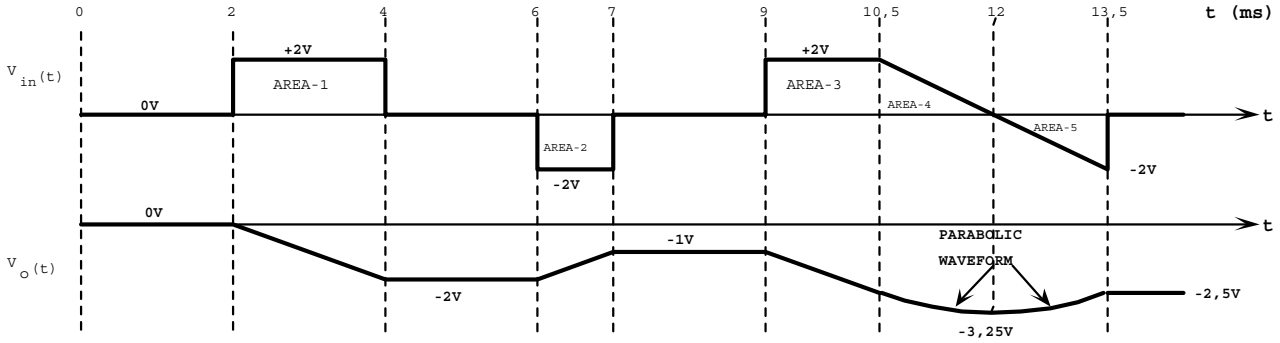
$$V_{o(t_2)} = -\left(\frac{1}{20K \times 0{,}1\mu}\right)\int_{t_1}^{t_2} V_{in(t)}\,dt + V_{o(t_1)} = -500\int_{t_1}^{t_2} V_{in(t)}\,dt + V_{o(t_1)}$$

Integration of a constant voltage (a):

$$\int a \times dt = a\,t + K \Rightarrow linear\ function, slope = a$$

Integration of a ramp voltage (at+b):

$$\int (a\,t + b)\,dt = 0{,}5\,a\,t^2 + b\,t + K \Rightarrow parabola$$



Interval	$V_{o(t_1)}$	$-500\int V_{in(t)}\,dt$ from t_1 to t_2	$V_{o(t_2)}$
0 to 2 ms	0	-500 x area = 0	0
2 to 4 ms	0	(area-1) -500 x (+2 x 2m) = -2	-2
4 to 6 ms	-2	-500 x area = 0	-2
6 to 7 ms	-2	(area-2) -500 x (-2 x 1m) = +1	-1
7 to 9ms	-1	-500 x area = 0	-1
9 to 10,5 ms	-1	(area-3) -500 x (+2 x 1,5m) = -1,5	-2,5
10,5 to 12 ms	-2,5	(area-4) -500 x (+2 x 1,5m x 0,5) = -0,75	-3,25
12 to 13,5 ms	-3,25	(area-5) -500 x (-2 x 1,5m x 0,5) = +0,75	-2,5
13,5 ms onward	-2,5	-500 x area = 0	-2,5

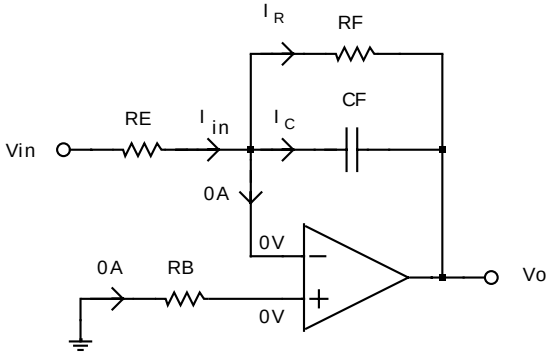
10. UNIDEAL INVERTING INTEGRATOR

$$\Delta V_o = V_{o(t_2)} - V_{o(t_1)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(AC)}\,dt \quad if \quad \omega \rangle \frac{10}{R_F C_F}$$

$$Z_{IF\ (ideal)} = \frac{V_{in}}{I_{in}} = R_E$$

$$Z_{OF\ (ideal)} = \left.\frac{V_o}{I_o}\right|_{V_{in}=0} = 0$$

$R_B = R_E \| R_F$ for minimum O/P DC offset.



The unideal integrator is actually a low-pass filter which can be used to integrate (and attenuate) HF signals and pass LF signals unattenuated with a gain of $A_{VF\ (LF)} = -R_F/R_E$. Low-frequency signals will not be integrated, therefore use the integration formula only for frequencies $\omega > 10/(R_F C_F)$ where $1/(R_F C_F)$ is the cutoff frequency of the filter in r/s.

Derivation of $V_o(t)$

$$dV_C = -dV_o = \frac{I_C}{C_F}\,dt \quad \Rightarrow \quad V_{o(t_2)} = -\left(\frac{1}{C_F}\right)\int_{t_1}^{t_2} I_C\,dt + V_{o(t_1)} \quad where \quad I_C = I_{in} - I_R = \frac{V_{in}}{R_E} - I_R$$

To integrate the input voltage waveform properly, the input current should be fully integrated by C_F but part of it is shunted by R_F . Therefore I_{in} will be integrated only if $I_C >> I_R$ which will occur only if the frequency of the input waveform is high enough such that the reactance of the capacitor is much smaller than R_F. For a periodic input signal, the following applies:

$$I_R = \frac{-V_o}{R_F} \quad and \quad I_C = \frac{-V_o}{1/\omega C_F} = -\omega C_F V_o \quad \Rightarrow \quad I_C \rangle\rangle I_R \quad \Rightarrow \quad -\omega C_F V_o \rangle\rangle \frac{-V_o}{R_F} \quad \Rightarrow \quad \omega \rangle\rangle \frac{1}{C_F R_F}$$

If $\omega >> (R_F C_F)^{-1}$, then $I_C \approx I_{in}$ and the following holds true.

$$V_{o(t_2)} = -\left(\frac{1}{C_F}\right)\int_{t_1}^{t_2} I_C\,dt + V_{o(t_1)} = -\left(\frac{1}{C_F}\right)\int_{t_1}^{t_2} I_{in(AC)}\,dt + V_{o(t_1)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(AC)}\,dt + V_{o(t_1)}$$

$$\Delta V_{o(PP)} = V_{o(t_2)} - V_{o(t_1)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(AC)}\,dt$$

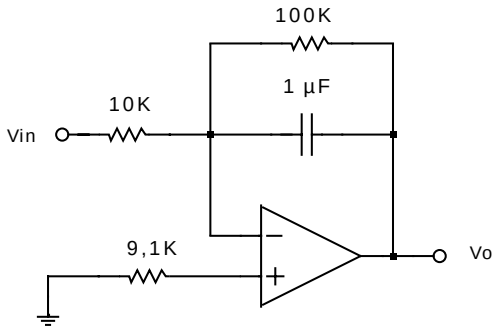
The formula beside can be used to determine the peak-to-peak amplitude of V_o provided that the interval t_1 - t_2 corresponds the <u>entire I/P waveform area</u> either above or below its DC component.

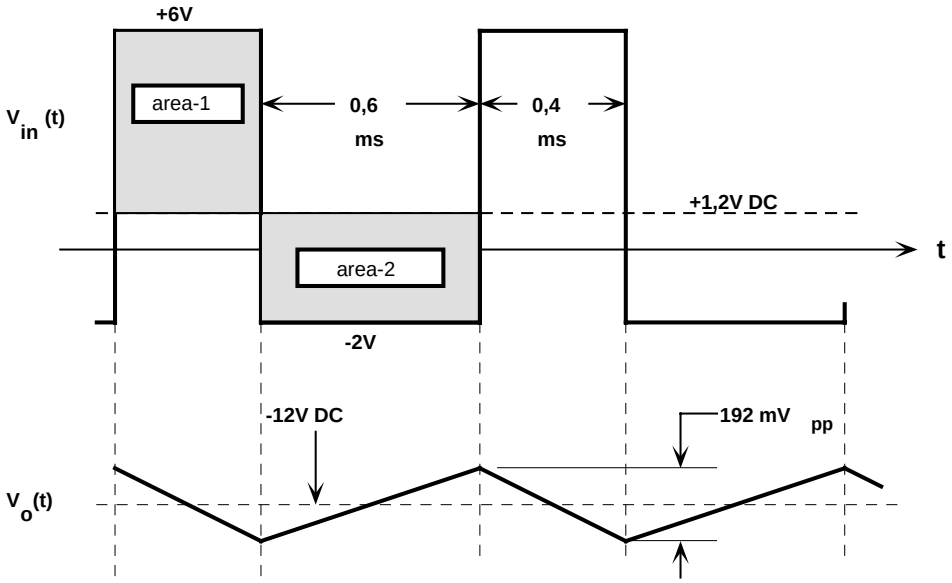
Notice that the DC component of V_{in} will never be integrated ($\omega = 0$ for DC) because the capacitor will block the DC component of I_{in} after 5 $R_F C_F$ and that DC component will flow through R_F. The steady-state DC analysis, after the initial transient of 5 $R_F C_F$, can be done simply by replacing C_F with an open circuit and analysing for V_o - the result can be predicted easily, $V_{in(DC)}$ will be amplified by the inverting gain of the circuit $A_{VF\ (DC)} = -R_F/R_E$.

NOTE: the above circuit will not saturate if there is no input signal as it was the case with the ideal integrator because any small DC leakage current will be shunted by R_F and will not flow through C_F which will keep the output at 0V DC .

Example: Integration of a periodic waveform

Determine the output waveform given the input waveform shown below assuming that the initial transient has already occurred - this means that C_F has fully charged to the final DC voltage and that it is blocking the DC component of I_{in}.





A) Calculation of the DC output.

The time average of a function over an interval t_1 to t_2 is given by the following expression:

$$V_{in(DC)} = V_{in(ave)} = \left(\frac{1}{t_2 - t_1}\right)\int_{t_1}^{t_2} V_{in(t)}\,dt$$

For a periodic function, the average of the function is the same over any one cycle of the function which translates into:

$$V_{in(DC)} = V_{in(ave)} = \frac{1}{T}\int_{t}^{t+T} V_{in(t)}\,dt$$

The average of a squarewave is therefore given by:

$$V_{in(ave)} = \frac{1}{T}\left[\int_0^{PW} V_{in}^{+}dt + \int_{PW}^{T} V_{in}^{-}dt\right] = \frac{1}{T}\left[V_{in}^{+}\int_0^{PW} dt + V_{in}^{-}\int_{PW}^{T} dt\right] = \frac{1}{T}\left[\left(V_{in}^{+}\times(t)_0^{PW}\right) + \left(V_{in}^{-}\times(t)_{PW}^{T}\right)\right]$$

$$V_{in(ave)} = \left(\frac{V_{in}^{+}}{T}(PW - 0)\right) + \left(\frac{V_{in}^{-}}{T}(T - PW)\right) = V_{in}^{+}\left(\frac{PW}{T}\right) + V_{in}^{-}\left(\frac{SW}{T}\right)$$

$$V_{in(ave)} = V_{in}^{+}\left(\frac{PW}{T}\right) + V_{in}^{-}\left(\frac{SW}{T}\right) = 6\left(\frac{0,4\,m}{1\,m}\right) + (-2)\left(\frac{0,6m}{1\,m}\right) = +1,2\,V \qquad V_{o(DC)} = -\frac{R_F}{R_E}V_{in(DC)} = -\frac{100k}{10k}\times 1,2 = -12V$$

B) Calculation of the AC output

The circuit will integrate the AC component of the input waveform only if

$$F \rangle \frac{10}{2\pi\, R_F C_F} = \frac{10}{2\pi\, 100k \times 1\mu} = 15{,}9\ Hz \quad \Rightarrow \quad F = 1\ kHz \rangle 15{,}9\ Hz$$ which is OK.

Therefore the formula $\Delta V_{o(PP)} = V_{o(t_2)} - V_{o(t_1)} = -\left(\frac{1}{R_E C_F}\right)\int_{t_1}^{t_2} V_{in(AC)}\,dt$ can be applied.

When V_{in} is above the DC level, we have:

$$\Delta V_{o(PP)} = -\left(\frac{1}{10K \times 1\mu}\right)\int_{0}^{PW} (6-1{,}2)\,dt = -(4{,}8 \times 0{,}4m) = -0{,}192\ V_{PP}$$

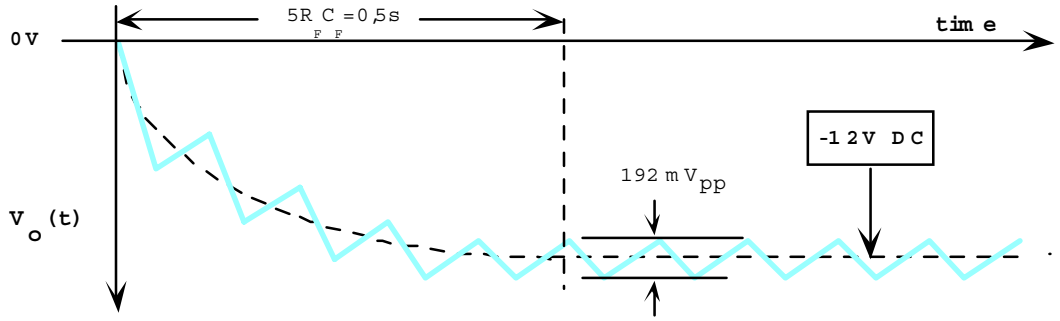
where the negative sign means that V_o goes down.

When V_{in} is below the DC level, we have:

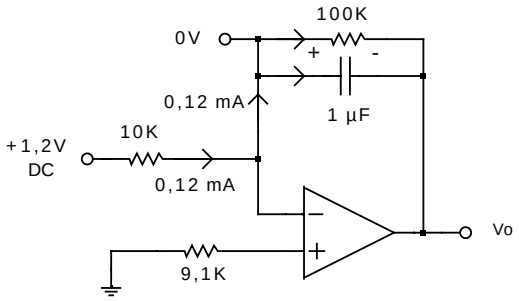
$$\Delta V_{o(PP)} = -\left(\frac{1}{10K \times 1\mu}\right)\int_{PW}^{T} (1{,}2-(-2))\,dt = -(-3{,}2 \times 0{,}6m) = +0{,}192\ V_{PP}$$

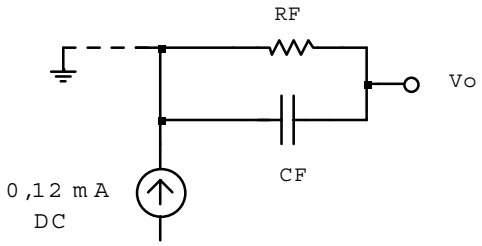
where the positive sign means that V_o goes up.

C) Initial transient



Initially, the DC voltage across C_F is 0V and will go down to -12V in five time constants.

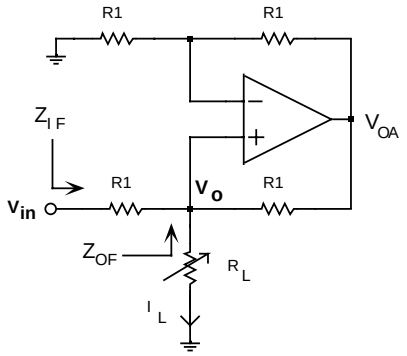




The 0,12 mA current is equivalent to a perfect DC current source driving the R_F C_F parallel combination, therefore C_F is charged to the final DC voltage (0,12m x R_F) in $5R_F$ C_F.

11. CURRENT SOURCES

Howland source



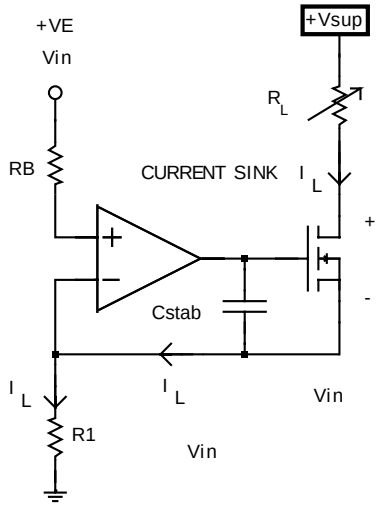
$$I_L = V_{in}/R_1$$

$$Z_{IF} = \frac{R_1}{1-(R_L/R_1)}$$

$$Z_{OF} = \infty$$

R_L is referenced to ground.
Load current cannot be high because it is supplied by V_{in} and the op amp output. V_{in} can be either DC or AC, which means I_L can also be DC or AC.

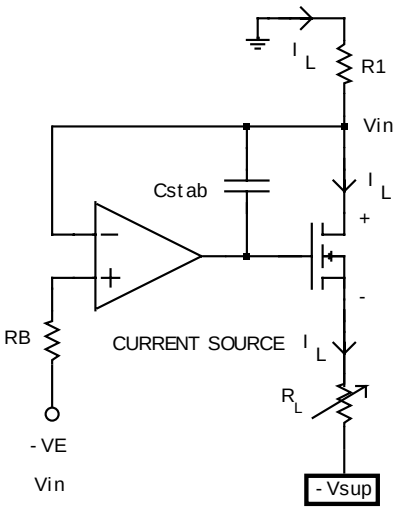
Current sink



$$I_L = V_{in}/R_1 \quad Z_{IF} = \infty \quad Z_{OF} = \infty$$

R_L is not referenced to ground.
Load current can be high if a power MOSFET is used. V_{in} has to be a positive DC voltage alone or with a superimposed AC voltage with a net AC+DC positive voltage.

Current source

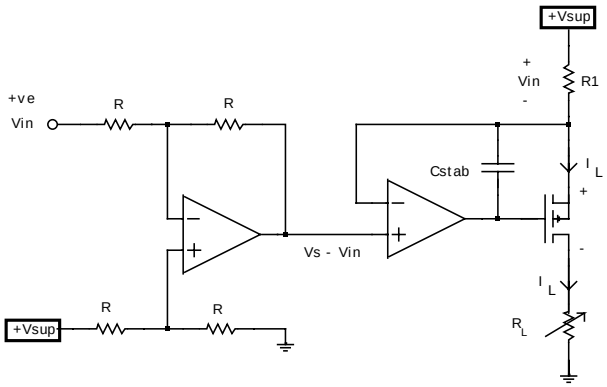


$$I_L = |V_{in}|/R_1 \quad Z_{IF} = \infty \quad Z_{OF} = \infty$$

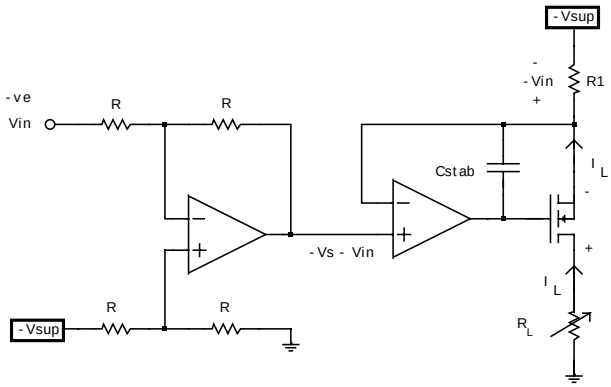
R_L is not referenced to ground.
Load current can be high if a power MOSFET is used. V_{in} has to be a negative DC voltage alone or with a superimposed AC voltage with a net AC+DC negative voltage.

Ground-referenced current sources

Current source



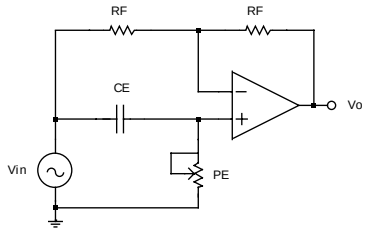
Current sink



The first stage of the above two circuits is a unity-gain subtractor used to generate V_{SUP}-V_{in} which is applied to the bottom of R_1 thus forcing V_{R1} to equal V_{in} and $I_L = V_{in}/R_1$. The MOSFET is used to boost the current capacity of the op amp. The inputs of the second op amp should be able to accommodate the voltage V_{sup}-V_{in} : if V_{sup}-V_{in} is close to V_{sup}, the input voltage range of the selected op amp must go right up to the supply rail..

12. Phase Shifters

Lead network

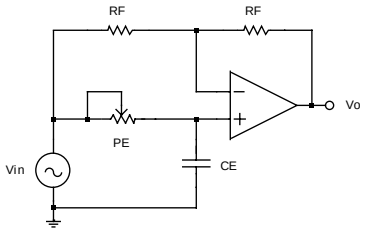


$$A_{VF} = \frac{P_1 + jX_C}{P_1 - jX_C}$$

$$|A_{VF}| = 1$$

$$\underline{/A_{VF}} = 2\arctan\frac{X_C}{P_1}$$

Lag network

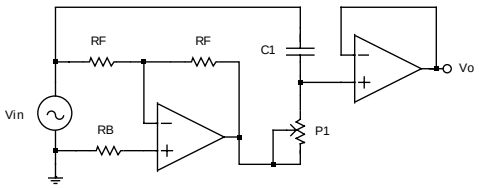


$$A_{VF} = \frac{-P_1 - jX_C}{P_1 - jX_C}$$

$$|A_{VF}| = 1$$

$$\underline{/A_{VF}} = \pi + 2\arctan\frac{X_C}{P_1}$$

Lead network



$$A_{VF} = \frac{P_1 + jX_C}{P_1 - jX_C}$$

$$|A_{VF}| = 1$$

$$\underline{/A_{VF}} = 2\arctan\frac{X_C}{P_1}$$

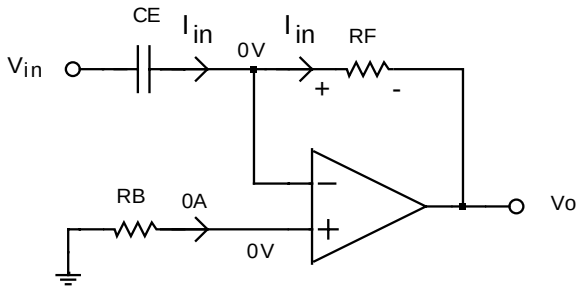
Since the magnitude of the gain is one, the output amplitude will always be equal to the input amplitude. The adjustment range of the phaseshift will depend on the size of P_1 and C and also on the frequency because X_C varies with frequency.

13. THE IDEAL DIFFERENTIATOR

Assuming an ideal op amp, we have:

$$I_{in} = C_E \frac{dV_{in}}{dt} \qquad V_o = -I_{in} R_F = -R_F C_E \frac{dV_{in}}{dt}$$

$R_B = R_F$ to balance input resistances in order to minimise the O/P DC offset.



Stability problem

The above circuit is not a stable one because of the phaseshift introduced by the feedback network :

$$V^- = V_o \times \left(\frac{-jX_{C_E}}{R_F - jX_{C_E}} \right)$$

phaseshift of V^- w.r.t. V_o varies from 0 to -90° over frequency

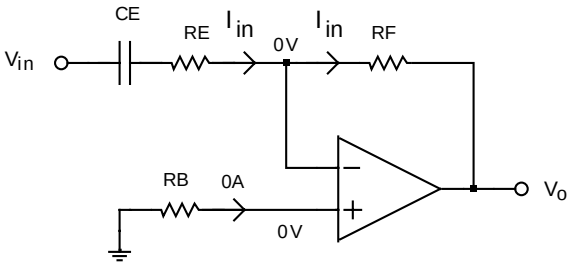
the op amp itself will introduce -180° because of the inversion, and internal compensation of the op amp introduces an additional -90°. Additional phaseshifts will be introduced by the internal circuit of the op amp at high frequencies. What all this means is that total phaseshift of the feedback loop will reach -360° at a particular frequency and if the loop gain is greater than 0 dB, the circuit will self-oscillate and will therefore be useless for differentiation of the input signal.

THE UNIDEAL DIFFERENTIATOR

If V_{in} is a periodic waveform and $X_{CE} >> R_E$, then most of V_{in} will be dropped across C_E, that is if X_{CE} >10 R_E, then

$$V_{in} = I_{in} R_E + I_{in}\left(-jX_{C_E}\right) \approx -jI_{in} X_{C_E} \quad \text{and}$$

$$I_{in} = C_E \frac{dV_{in}}{dt} \qquad V_o = -I_{in} R_F = -R_F C_E \frac{dV_{in}}{dt}$$



Periodic input signal

The above circuit will differentiate the input signal only if $V_{R_E} \langle\langle V_{C_E}$ which occurs at

$$F_{in} < 0{,}1/(2\pi R_E C_E).$$

Aperiodic input signal

The above circuit will differentiate the input signal only if $V_{R_E} \langle\langle V_{C_E}$ which occurs if

$$I_{in} R_E \approx \left(C_E \frac{dV_{in}}{dt} \right) R_E = R_E C_E \frac{dV_{in}}{dt} \langle \frac{V_{in}}{10}$$

Design procedure

Given the following design parameters, determine the components using the procedure.

Input signal: maximum frequency F_{max} and maximum rate of change $(dV_{in}/dt)max$
Output signal: maximum amplitude V_o max
Op amp: minimum values of saturation voltage, gain-bandwidth product (GBW) and current limit.

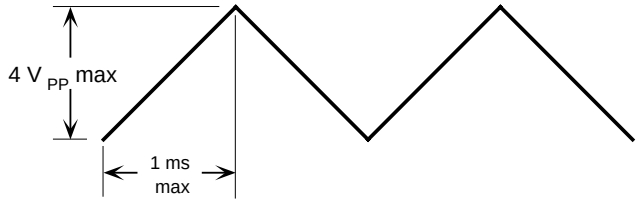
1. Determine C_E max necessary to keep the output current of the op amp to less than half of its minnimum current limit:	$I_{OPA(\max)} = C_E\left(\frac{dV_{in}}{dt}\right)_{\max} \Rightarrow C_E \langle \frac{I_{\lim(\min)}/2}{(dV_{in}/dt)_{\max}}$
2. Select C_E R_E combination that meets the differentiation criterion - select C_E R_E close to limit for maximum output voltage.	$F_{\max} \langle (20\pi C_E R_E)^{-1} \Rightarrow C_E R_E \langle (20\pi F_{\max})^{-1}$
3. Determine R_F max for a stable differentiator circuit - no ringing in O/P waveform.	$R_F \langle R_E[(0,5\pi C_E R_E GBW_{\min}) - 1]$
4. Select R_F required for a given maximum O/P voltage. If R_F exceeds limit of step 3, circuit will be unstable, therefore reduce R_F to calculated limit and add amplifier required to produce required maximum O/P amplitude.	$\lvert V_{o(\max)}\rvert = C_E R_F\left(\frac{dV_{in}}{dt}\right)_{\max}$

Example: Design and analysis of differentiator

A) Design a stable differentiator that is used to differentiate a triangular wave whose amplitude and frequency range are 0 to 4 V_{PP} and 0 to 500 Hz respectively. Assume that an LF347 op amp is used with ±15V supply voltages.

LF347: GBW > 1 MHZ, $|V_{SAT}|$ > 12V and minimum current limit ±10 mA (source and sink).

The maximum slope of the input signal will occur when both the amplitude and the frequency are maximum, that is at 4 V_{PP} and 500 Hz.



Input waveform

$$\left(\frac{dV_{in}}{dt}\right)_{\max} = \pm\frac{4}{1m} = \pm 4000\ V/s$$

1. $C_E \langle \frac{I_{\lim(\min)}/2}{(dV_{in}/dt)_{\max}} = \frac{10m/2}{4000} = 1{,}25\,\mu F$ maximum C_E

2. $C_E R_E \langle (20\pi F_{\max})^{-1} = (20\pi\, 500)^{-1} = 31{,}83\,\mu s$
Let $C_E R_E$ = 30 µs - close to limit for maximum output voltage. C_E =10 nF and R_E = 3K

3. For stability $R_F \langle R_E\left[(0{,}5\pi\, C_E R_E GBW_{\min}) - 1\right] = 3K \times \left[(0{,}5\pi\, 30\mu \times 1M) - 1\right] = 138{,}4K$

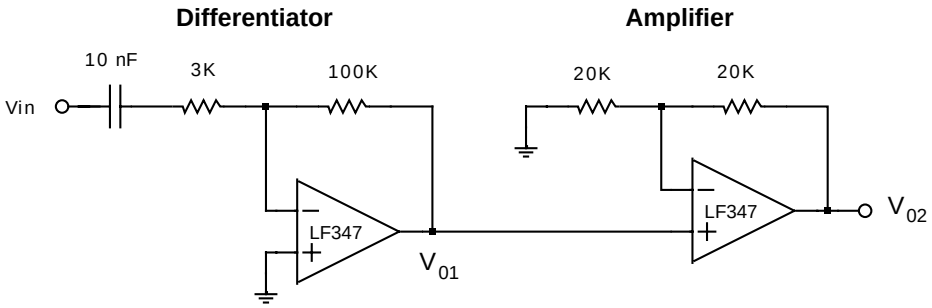
4. maximum O/P $|V_{o(\max)}| = C_E R_F \left(\frac{dV_{in}}{dt}\right)_{\max} \Rightarrow R_F = \frac{|V_{o(\max)}|}{C_E\left(\frac{dV_{in}}{dt}\right)_{\max}} = \frac{8}{10n \times 4000} = 200K$

Maximum O/P cannot be achieved with differentiator alone because circuit would be unstable, therefore let R_F = 100K for a stable circuit and then add an amplifier to obtain $8V_P$ max.

Differentiator O/P $|V_{o(\max)}| = C_E R_F \left(\frac{dV_{in}}{dt}\right)_{\max} = 10n \times 100K(4000) = 4V_P$

Amplifier gain must be $8V_P / 4V_P$ = 2 V/V Let's use an non-inverting amp with $R_F = R_E$ = 20K

Final circuit



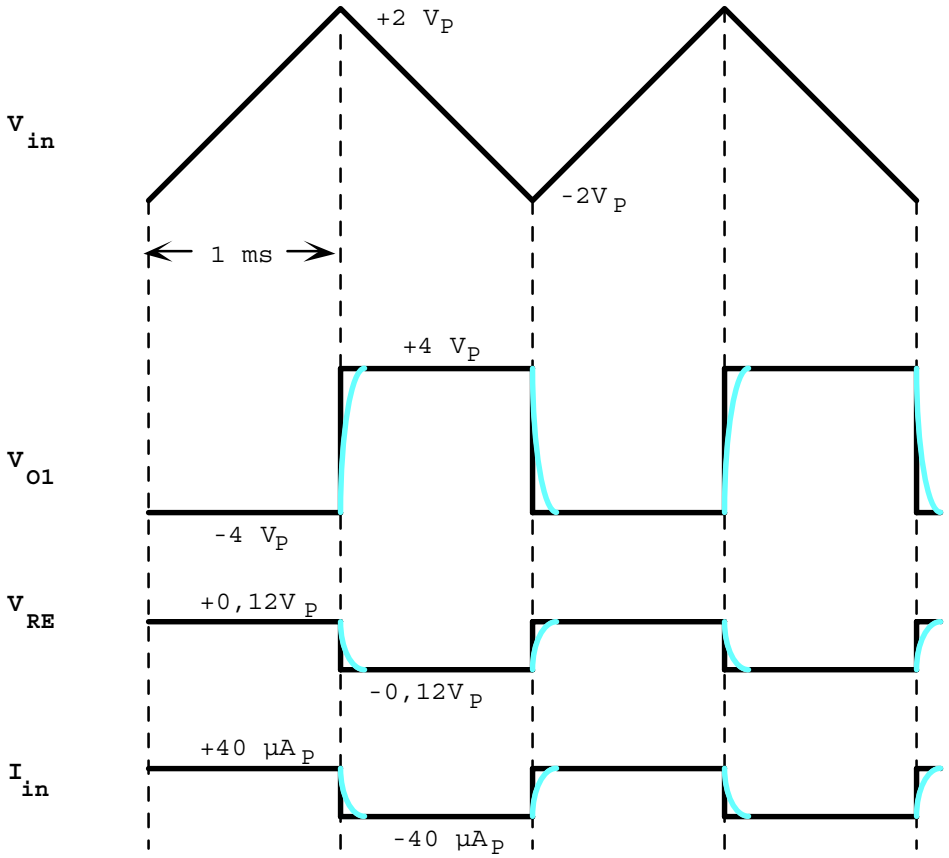
B) Determine the waveforms V_{o1}, I_{in} and V_{RE} relative to V_{in} for a 500 Hz and 4 V_{PP} triangular wave input.

$$V_o = -C_E R_F \left(\frac{dV_{in}}{dt}\right)_{\max} = -10n \times 100K \times (\pm 4000) = \mp 4V_P$$

$$I_{in} = C_E\left(\frac{dV_C}{dt}\right) \approx C_E\left(\frac{dV_{in}}{dt}\right) = 10n \times (\pm 4000) = \pm 40\,\mu A \qquad \text{if } V_{in} \approx V_{CE}$$

$$V_{R_E} = I_{in} R_E = \pm 40\,\mu \times 3000 = \pm 0{,}12V_P$$

Waveforms



The above waveforms are valid for V_{in} >> V_{RE} which is true for most of the input waveform voltages except when V_{in} is close to zero volt because V_{RE} is ±0,12V_P . The actual waveforms for $V_{O,}$ I_{in} and V_{RE} will have very short exponential edges (non-zero rise and fall times) instead of straight vertical edges (zero rise and fall times) as shown above. One can show that the 10%-90% rise and fall times of V_{01} is given by the following:

$$t_r = t_f = 2{,}2\, C_E R_E = 2{,}2 \times 10n \times 3000 = 66\ \mu s$$

which is negligible compared to the half period of 1 ms. Therefore the waveforms can be assumed to be good squarewaves.