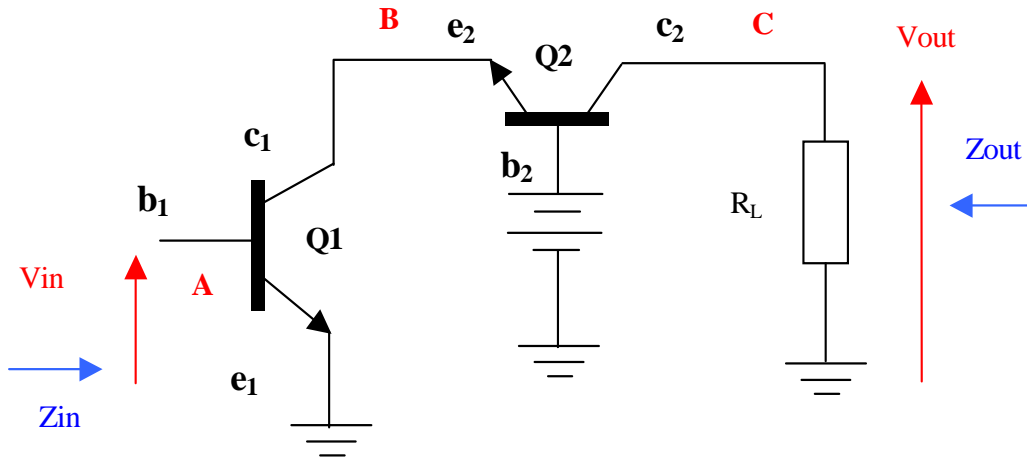


**Cascode BJT Circuit**

A popular circuit for use at high frequencies is the cascode amplifier, as shown below:-



Gain of Q1 due to load of Q2

$$\text{CE gain} = -g_{m1}R_{L1} \quad R_{IN} (\text{CB stage}) = \frac{1}{g_{m2}}$$

$$\therefore A_{V1} = -g_{m1} \frac{1}{g_{m2}} \text{ which assuming transistors are matched} = 1$$

$$A_{i1} = -\beta$$

Miller capacitance

$$C_{\text{SHUNT}} = C_{\text{BC}}(1 - A_v) = C_{\text{BC}}(1 - (-1)) \quad C_{\text{SHUNT}} = 2C_{\text{BC}}$$

The miller capacitance across the input of the CE stage is double the Base collector capacitance of Q1.



### Input Impedance

of Q1 at point A is

$$R_{IN} = \frac{\beta}{gm} \quad \text{where } gm = \frac{I_{CQ}}{V_T} ; \quad V_T = \frac{k \cdot T}{q} \quad \text{where } k = \text{Boltzmann's constant} = 1.3807 \times 10^{-23} \text{ JK}^{-1}$$

$q = \text{Electron charge} = 1.6022 \times 10^{-19} \text{ C}$

$T = \text{Temperature in Kelvin}$

$gm = \text{Transconductance (mS)}$

### Voltage Gain $A_v$

Voltage gain of CE stage is  $\sim 1$  (due to low output RL) so the voltage gain of the amplifier will be from the common-base stage:

$$A_v = \frac{V_{OUT}}{V_{IN}} = \frac{\beta_2 \cdot i_{b2} \cdot R_L}{i_{b2} (\beta_2 + 1) r_{be2}} = \frac{\beta_2 \cdot R_L}{(\beta_2 + 1) r_{be2}} \approx \frac{R_L}{r_{be}} = \frac{I_{CQ}}{V_T} \cdot \frac{V_A}{I_{CQ}} = \frac{V_A}{V_T} \quad \left( \text{as } \frac{1}{gm} = r_{ce} \right)$$

### Current Gain $A_i$

Current gain of CB stage is  $\sim 1$  so the current gain of the amplifier will be from the common-emitter stage.

Current gain ( $A_i$ ) =  $A_i$  of the CE stage ( $A_i$  of CB stage = 1) =  $\beta$

### Output Impedance

$R_{OUT} = R_L$

Of course as the voltage gain of the whole amplifier is dependant on the load resistor (and ultimately  $r_{ce2}$ ), then adding an active load (eg current mirror) will allow high voltage gain.



**Cascode Simulation**

For comparison a common-emitter stage was simulated on ADS to measure voltage gain.

Using the HF3127B transistor array we can calculate the voltage gain of the circuit at low frequencies. If we assume a supply voltage of 5V and a device current of 5mA, we can calculate the value of the load resistor (We also assume that we want half the supply voltage across the device so that  $V_C = 2.5V$ ).

$$R_L = \frac{V_{CC} - V_C}{I_{CQ}} = \frac{5 - 2.5}{5 \times 10^{-3}} = 500 \Omega$$

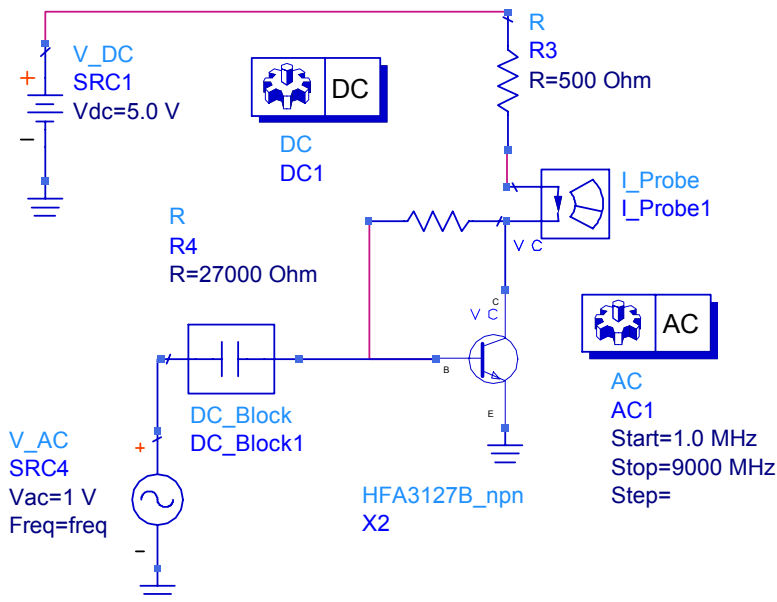
Device Data  $V_A = 50V$ ;  $V_T = 25mV$ ;  $\beta = 100$

$$AV = -gm.R_L = -\frac{V_T}{I_{CQ}}.R_L = -\frac{25 \times 10^{-3}}{5 \times 10^{-3}}.500 = 2500 \text{ in dB's} = 10 * \log(2500) = 34 \text{ dB}$$

$$\text{Base collector bias resistor} = \frac{V_C - V_{be}}{I_{CQ}/\beta} = \frac{2.5 - 0.7}{5 \times 10^{-3}/100} = 36 \text{ K}\Omega$$

At low frequencies we would expect a voltage gain of 34dB rolling off to a gain of 0dB at the  $f_T$  of the device (~ 8GHz).

Below is shown the simulation and result from ADS.



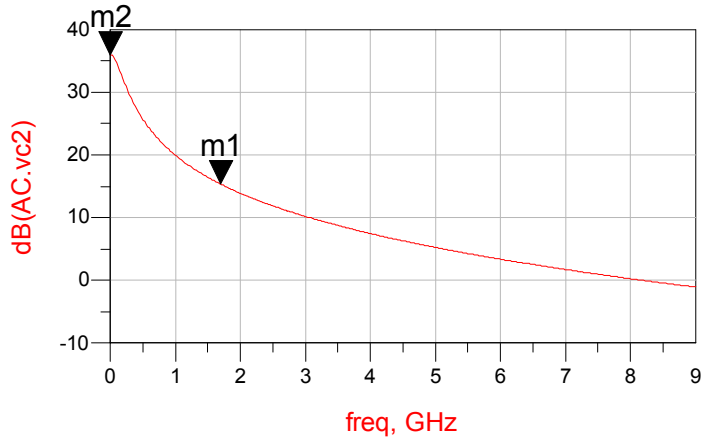
Note a DC block is used as the AC source has a DC of 0V. During simulation the value of the base-collector resistor was reduced to ensure  $I_C = 5mA$ .

And the resulting data of voltage gain vs frequency for the single-stage common-emitter amplifier.

|         |               |
|---------|---------------|
| DC.vc2  | DC.I_Probe1.i |
| 2.289 V | 5.423mA       |

m2  
freq=1.000MHz  
dB(AC.vc2)=35.944

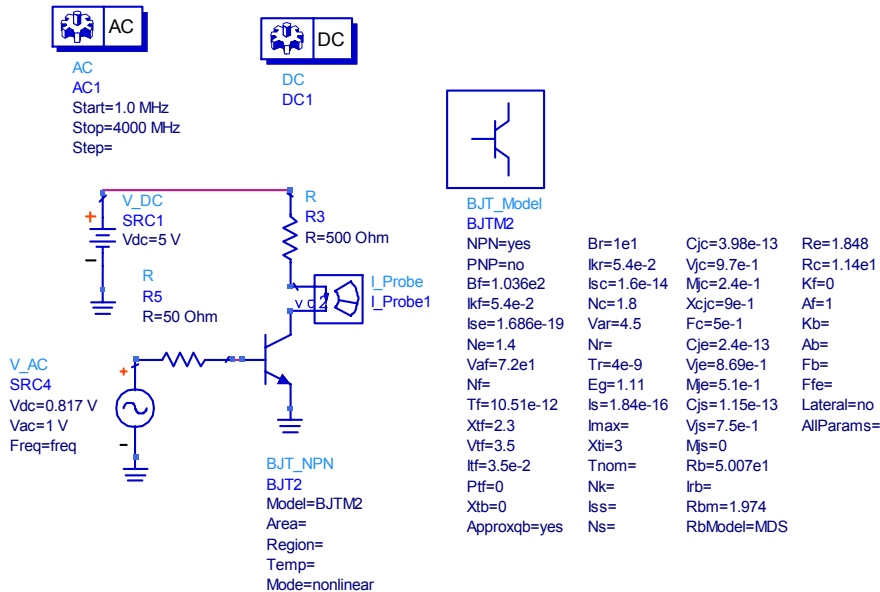
m1  
freq=1.696GHz  
dB(AC.vc2)=15.335



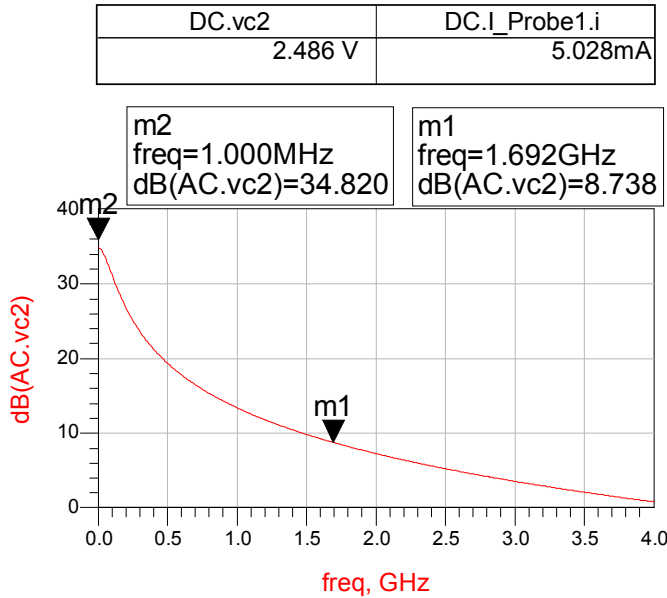
The predicted low-frequency voltage gain agrees well with our initial calculation.

However, we have not included a source resistance – this will effectively form a potential divider with the base bulk resistor  $r_b$ , and lower the voltage entering the device and hence lowering the gain.

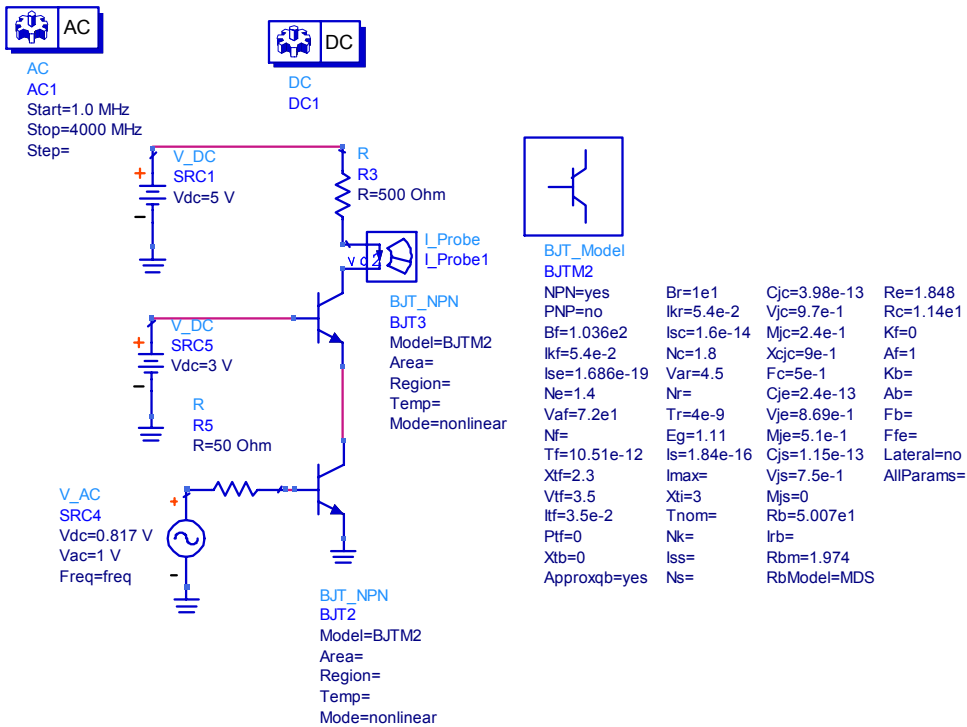
Now a 50-ohm resistor has been added to the ideal input voltage source.



The resulting plot now shows how gain has rolled off faster due to the Miller effect.



To improve the high frequency response and stability we now add a common-base stage to form a Cascode amplifier. The common-base stage is biased in saturation and therefore there will be little voltage drop across the collector-emitter junction.





The red plot shows the voltage gain of the CE stage showing that the gain of the first stage is now a lot lower than the single CE stage amplifier. The blue plot shows the new voltage gain response of the Cascode amplifier and at marker 2 (1.69GHz) the gain has improved from 8.7dB to 12.6dB, as the Miller effect has been reduced.

|         |               |
|---------|---------------|
| DC.vc2  | DC.I_Probe1.i |
| 2.528 V | 4.944mA       |

|  |
|--|
| m1<br>freq=1.000MHz<br>dB(AC.vc2)=34.935 |
|--|

|  |
|--|
| m2<br>freq=1.692GHz<br>dB(AC.vc2)=12.631 |
|--|

