PIR CONTROLLER

GENERAL DESCRIPTION 功能敘述

The M7610A is a CMOS LSI designed for automatic PIR lamp control. It can operating with 2 wire configurations for triac applications or with 3 wire configurations for relay applications. The chip contains operational amplifiers, comparator, timer, a zero crossing detector, a control circuit, a voltage regulator, a system oscillator and an output timing oscillator.

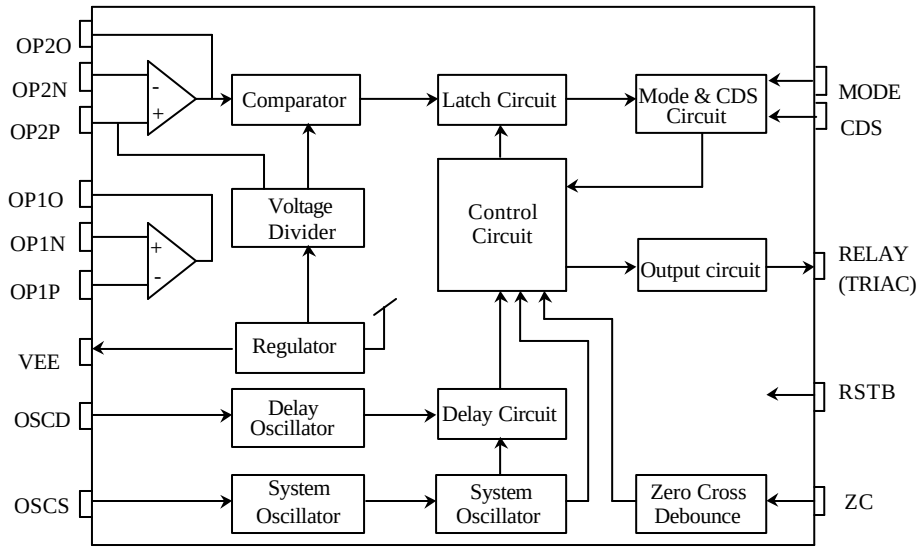
FEATURES 產品特長

- On-chip regulator.
- Adjustable output duration.
- CDS input.
- 30 second warm-up.
- ON/AUTO/OFF selected by MODE pin.
- Override function.
- Auto-reset if the ZC signal disappears for over 3 second.
- 16 pin DIP or SOP package.

APPLICATIONS 產品應用

- PIR light controller, Motion Detector, Alarm system, Auto-door bell.

BLOCK DIAGRAM 功能方塊圖



PIR CONTROLLER

ABSOLUTE MAXIMUM RATING

(TA=25℃)

Parameter	Rating	Unit
Supply Voltage	-0.3 to 13.0	V
Input Voltage	V_{SS}-0.3~V_{DD} +0.3	V
Operating Temperature	-25 to 75	℃
Storage Temperature	-50 to 125	℃
Zero Crossing Current	Max 300	μA

ELECTRICAL CHARACTERISTICS

Characteristics	Sym.	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	5	9	12	V	
Regulator Output Voltage	V_{EE}	3.5	4	4.5	V	V_{DD}– V_{EE}
Operating Current	I_{DD}	—	100	350	μA	No load, OSC on.
CDS “H” Transfer Voltage	V_{TH1}	6.4	8	9.6	V	
CDS “L” Transfer Voltage	V_{TH1}	3.7	4.7	5.6	V	
Output Source Current(Relay, Triac)	I_{OH1}	-6	-12	—	mA	V_{OH} = 10.8V
Output Sink Current(Relay, Triac)	I_{OL1}	40	80	—	mA	V_{OL} = 1.2V
VEE Sink Current	I_{OL2}	—	1	—	mA	VDD-VEE=4V
“H” Input Voltage	V_{IH}	0.8 V_{DD}	—	—	V	
“L” Input Voltage	V_{IL}	—	—	0.2 V_{DD}	V	
ZC “H” Transfer Voltage	V_{TH2}	4.7	6.7	8.7	V	
ZC “H” Transfer Voltage	V_{TH2}	4.7	6.7	8.7	V	
ZC “L” Transfer Voltage	V_{TL2}	1.3	1.8	2.3	V	
System Oscillator Frequency	F_{SYS}	12.8	16	19.2	KHz	Rosc=680KΩ, Cosc=100P (RELAY) Rosc=620KΩ, Cosc=100P (TRIAC)
Delay Oscillator Frequency	Fd	1.28	1.6	1.92	KHz	Roscd=270K,C_{OSCD}=3900P
OP Amp Open Loop Gain	A_{VO}	60	80	—	dB	No load
OP Amp Input Offset Voltage	Vos	—	10	35	mV	No load

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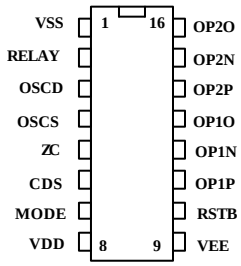
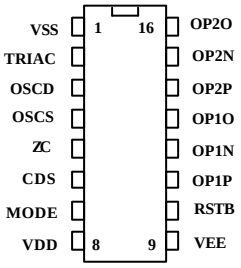
Pin Assignment





Pin Description

Pin No		Pin Name	Description
A	B		
1		VSS	Negative power supply.
2		RELAY	Relay drive output through external NPN transistor. Active high.
	2	TRIAC	Triac drive output. Pulse output when active.
3	3	OSCD	Delay time oscillator I/O pin.
4	4	OSCS	System oscillator I/O pin.
5	5	ZC	Input pin for AC zero crossing detecting.
6	6	CDS	Connect to the CDS voltage divider for daytime/night auto-detecting.
7	7	MODE	Operating mode selection input.
8	8	VDD	Positive power supply.
9	9	VEE	Regulated voltage output pin.
10	10	RSTB	Chip reset input pin. Active low.
11	11	OP1P	Noninverting input of OP1.
12	12	OP1N	Inverting input of OP1.
13	13	OP1O	Output of OP1.
14	14	OP2P	Noninverting input of OP2.
15	15	OP2N	Inverting input of OP2.
16	16	OP2O	Output of OP2.

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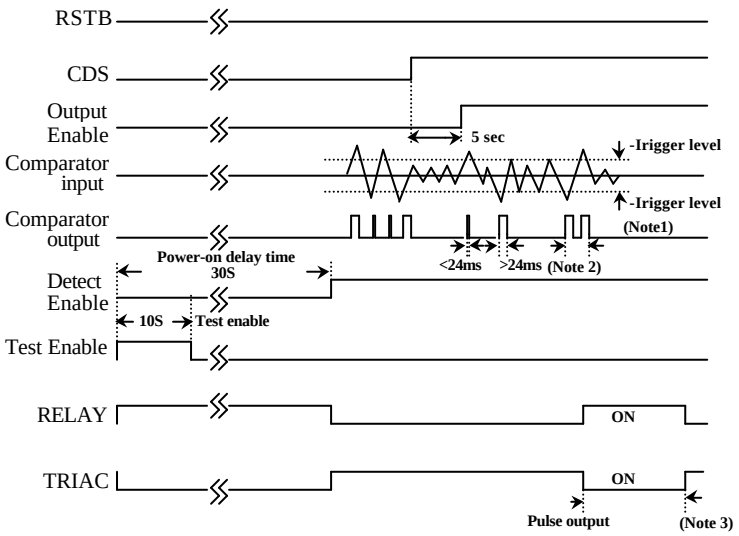
Trigger Timing



Note :

1. The output will be activated, if the trigger signal meets the following criteria:
   - 3 triggers within 2 seconds.
   - A trigger signal sustain duration≧0.34s.
   - 2 trigger signals within 2s with one of the trigger signal sustain≧0.16s.
2. The effective comparator output width can be selected to be 24ms or 32ms or 48ms by mask option, the default is 24ms (system frequency = 16KHz).
3. The output duration is set by external RC connected to the OSCD pin.

Functional Description

- **VEE :**

  The VEE supplies power to the analog front end circuits with a stabilized voltage which is –4V with respect to VDD normally.

- **OSCS :**

  System oscillator input pin, connect to external RC to generate 16KHz system frequency.

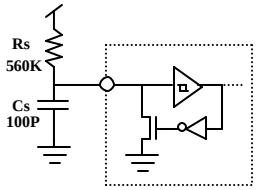


Fig.1 System oscillator

- **OSCD :**

  Output timing oscillator input pin, connect to external RC to obtain desired output turn-on duration. Variable output turn-on duration can be obtained by selecting various values of RC or using a variable resistor.

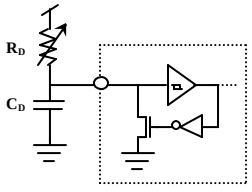


Fig.2 Output timing oscillator

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· **RELAY (TRIAC) :**

The output pin is set as a relay driving (active high) output for the M7610A, or as a triac driving (active low)output for the M7610B. The output active duration is controlled by the OSCD oscillating period.

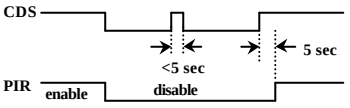
	M7610A	M7610B
OUTPUT	Relay	Triac

· **CDS :**

This pin is a CMOS Schmitt trigger input structure. It is used to distinguish between day time & night. When the input voltage of CDS is high the PIR input will be enabled.

When CDS is low the PIR input will be disabled. The input disable to enable debounce time is 5 seconds. Connect this pin to VDD when not using this function.

CDS	Status	PIR
LOW	Day time	Disable
HIGH	Night	Enable



· **MODE :**

This tri-state input pin is used to select the operating mode.

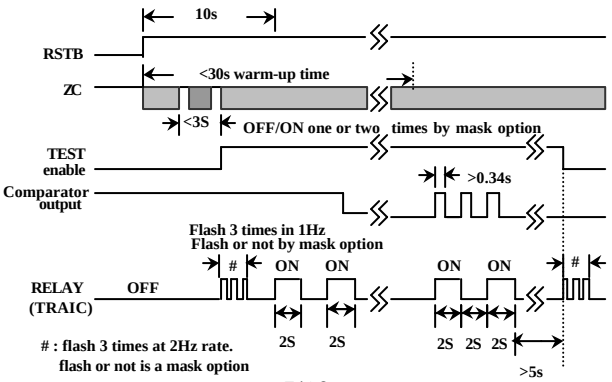
MODE Status	Operating Mode	Description
VDD	ON	Output always ON: RELAY pin output high for relay driving. TRIAC pin pulse train output synchronized by ZC for triac driving.
VSS	OFF	Output always OFF: RELAY pin output low for relay driving. TRIAC output high for triac driving.
OPEN	AUTO RELAY (TRIAC)	Outputs remain in off state, until activated by a valid PIR input trigger signal. When working in AUTO mode, the chip allows override control by switching the ZC signal.

· **ZC :**

this pin is a CMOS input structure. It receives AC line frequency and generates zero crossing pulses to synchronize the triac driver. By effective ZC signal switching (switch OFF/ON 1 or 2 times within 3 seconds, by mask option), the chip provides following additional functions:

- Test mode control :

  Within 10 seconds after power-on, effective ZC switching will force the chip to enter the test mode. During the test mode, the outputs will be active for 2 seconds duration each time when triggered by a valid PIR trigger signal. If there is a time interval of more than 5s without a valid trigger input, the chip will go to AUTO automatically.



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- Override control**:**

  when the chip is working in AUTO mode (MODE= open), the output will be activated by a valid PIR trigger signal and the output active duration controlled by the OSCD oscillating period. The lamp can be switched to always on from the AUTO state by either switching the MODE pin to VDD or switching the ZC signal by an OFF/ON operation of the power switch (OFF/ON 1 or 2 times within 3 second by mask option). The term override here means changing the operating mode by switching the power switch. The chip can be toggled from ON to AUTO by an override operation. If the chip is overridden to ON and there is no further override operation, it will return to AUTO automatically after an internal preset ON time duration has elapsed. This override ON time duration can be selected to be 4 or 6 or 8 hours by mask option. The default is 8 hours. The chip offers a mask option for selecting an output flash (3 times)or not when changing the operating mode. It will flash 3 times at a 1Hz rate every time when the IC changes from AUTO to another mode and flash 3 times at a 2Hz rate when returning to AUTO mode. However it will not flash if the mode is changed by switching the MODE switch.

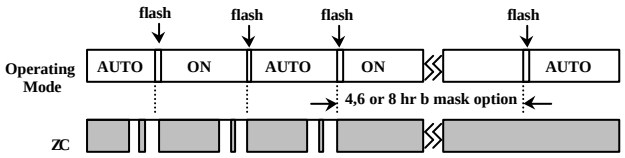

Fig.3 ZC overidde timing

- **RSTB :**

  This pin is used to reset the chip. Internal pull-high, active low. Fig4 shows an RSTB application example. The use of C_{RST} can extend the power-on initial time. If the RSTB pin is open circuit (Without C_{RST}), the initial time is equal to the default (30s).

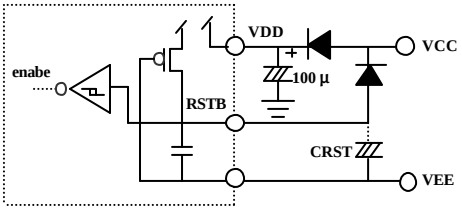

Fig.4 RSTB application example

- **Power on initial :**

  The PIR signal amplifier needs a warm up period after power-on, so during this time the input should be disabled. In AUTO mode within the first 10 seconds of power-on initial, the chip allows override control to enter the test mode. After 30 seconds of initial time it allows override control between ON and AUTO. The chip will remain in the warm up period if the total initial time was not elapsed after return to AUTO. Incase the ZC signal disappears for more than 3 seconds, it will restart the initial operation. However the restarted initial time is always 30 seconds and cannot be extended by adding C_{RST} to the R_{STB} pin as shown in Fig 4.

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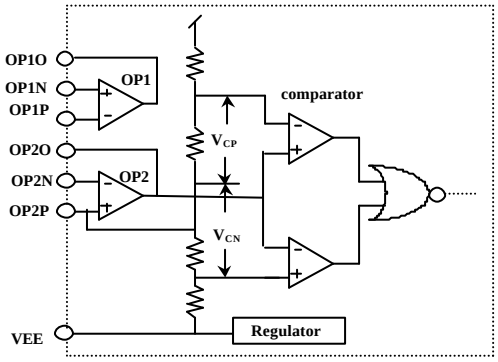

Fig.5 PIR amplifier block diagram

- **Mask Options :**
  - 4,6 or 8 hours option to automatically return to AUTO from override ON. The default is 8 hours.
  - Option for effective override : 1 or 2 times OFF/ON operation of the power switch within 3 second. The default is 1times OFF/ON.
  - Option for output flash or not to indicate effective override operation. The default is to no flash.
  - Option for effective PIR trigger pulse width : > 24mS, > 32mS or >48mS. The default is 24ms.
  - Option for setting comparator window to be 1/16, 1/11.3 or 1/9 (VDD-VEE). The default is 1/16 (VDD-VEE).

- **PIR amplifier :**

Consult the diagram below for details of the PIR front end amplifier. In Fig.5 there are 2 op-amps with different applications. OP1 can be used independently as a first stage inverting or non-inverting amplifier for the PIR. As the output of OP2 is directly connected to the input of the comparator, therefore it is used as a second stage amplifying device. The non-inverting input of OP2 is connected to the comparator' s window center point and can be used to check this voltage and to provide a bias voltage that is equal to the center point voltage of the comparator. In Fig.5 the comparator can have 3 window levels, set by mask options,

1) 1/16 (VDD-VEE),

2) 1/11.3 (VDD-VEE),

3) 1/9 (VDD-VEE).

If not specified the default window will be set to 1/16 (VDD-VEE). The preset voltage for VDD-VEE is 4V. The V_{CP} and V_{CN} default value is therefore 0.25V,. (4/16 V)

- **Second stage amplifier :**

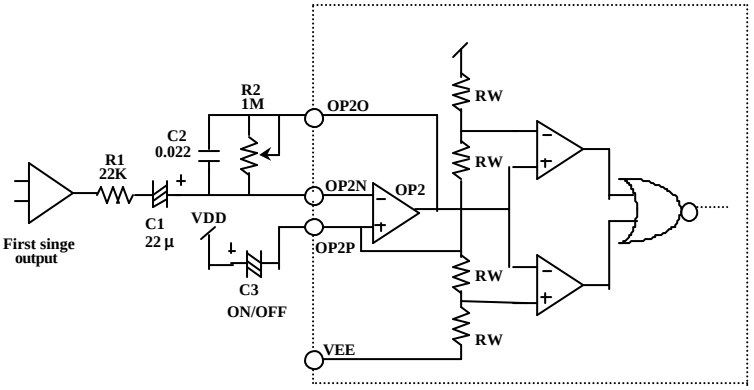

Fig. 6 Typical second stage amplifier

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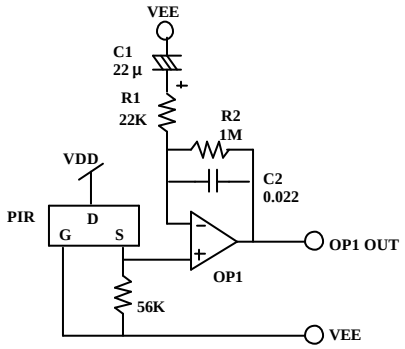

Fig.7 Typical PIR amplifier

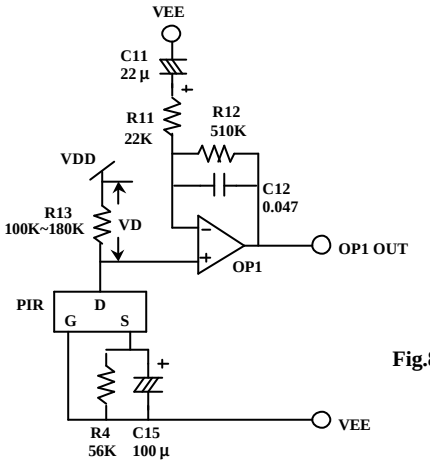

Fig.8 High gain first stage

Usually the second stage PIR amplifier is a simple capacitively coupled inverting amplifier with low pass configuration. In Fig.6 OP2P is directly connected to the comparator window center, and with the C3 filter can act as the bias for OP2. For this configuration AV=R2/ R1, low cutoff frequency

FL=1/2π R1C1, high cutoff frequency Fh=1/2π R2C2.By changing the value of R2 the sensitivity can be varied. C1 and C3, must be low leakage types, to prevent the DC operating point from changing due to current leakage.

- **Fist Stage of PIR amplifier :**

Fig.7 shows a typical first stage amplifier. C2 and R2 form a simple low pass filter with cut off frequency of 7Hz. The low frequency response will be governed by R1 and C1 with cut-off frequency at 0.33Hz. AV=(R1+R2)

Fig.7 and Fig.8 are similar but in Fig.8 the amplifier' s input signal is taken from the drain of the PIR. This has higher gain than Fig.7. Since OP1 is PMOS input V_D must be greater than 1.2V for adequate operation.

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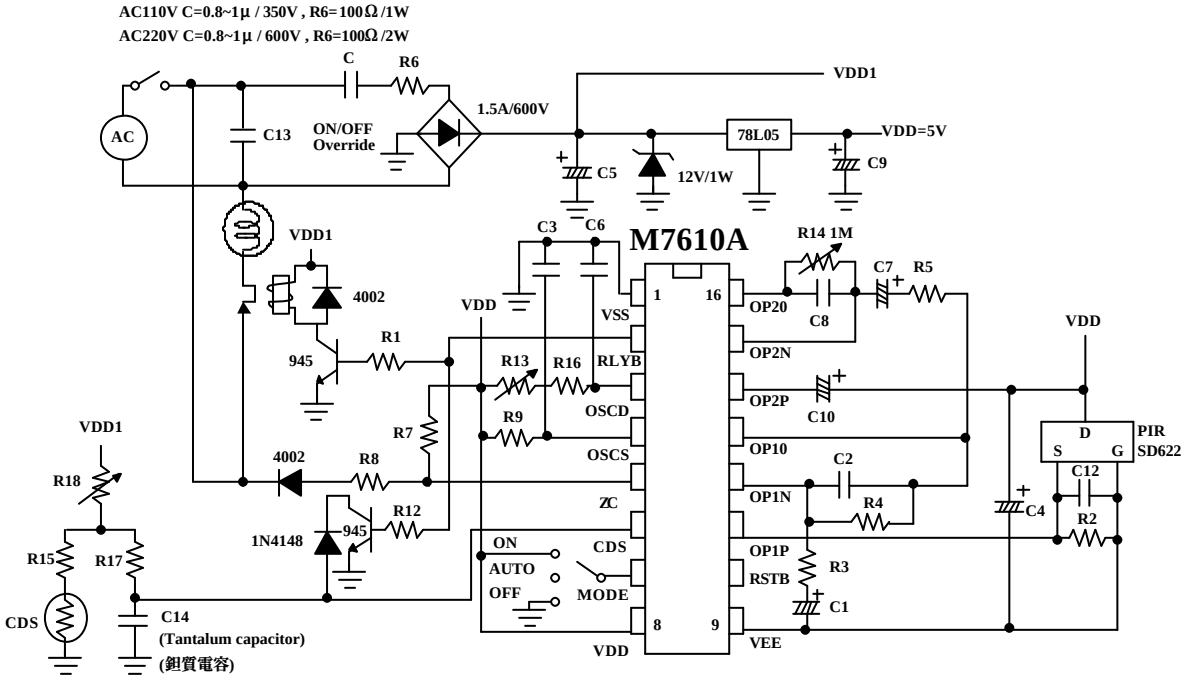
一.Relay Application



R1	22K	C1	22μ/16V
R2	56K	C2	0.022μ
R3	22K	C3	100P
R4	1M	C4	100μ/16V
R5	22K	C5	1000μ/16V
R6	100/2W	C6	0.01μ
R7	2.2M	C7	22μ/16V
R8	1M	C8	0.022μ
R9	680K	C9	330μ/16V
R12	100K	C10	10μ/16V
R13	1M	C12	0.022μ
R14	1M	C13	0.1μ/400~600V
R15	1.5K	C14	4.7μ
R16	47K		
R17	1M		
R18	30K		

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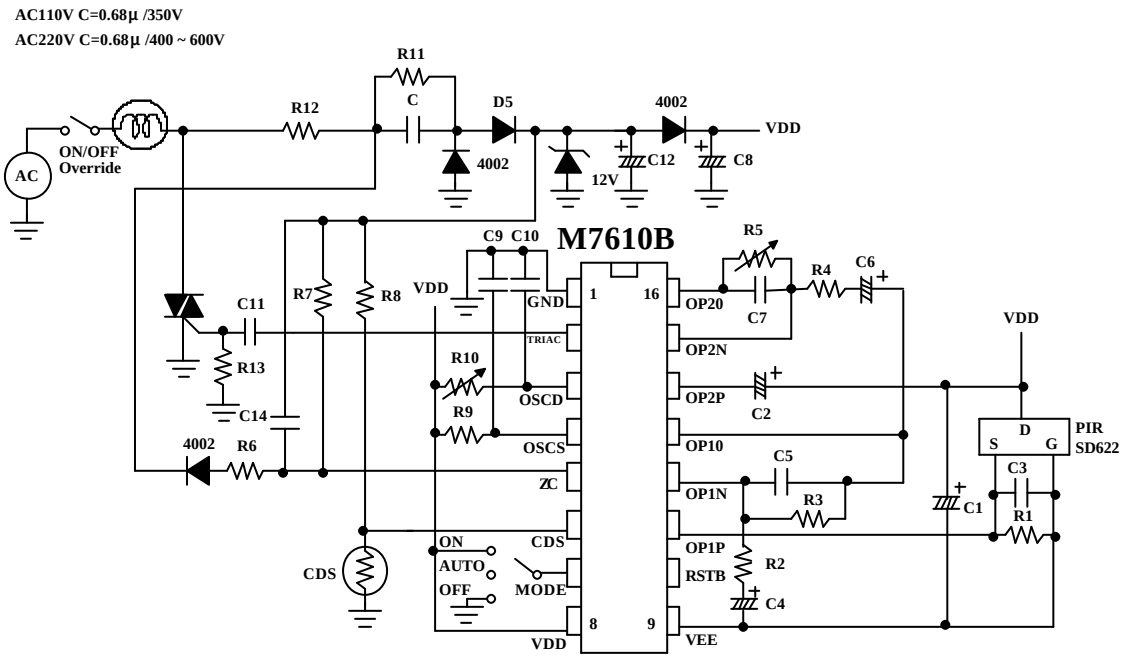
二. TRIAC Application



R1	100K	C1	100μ/16V
R2	22K	C2	10μ/16V
R3	1M	C3	0.022μ
R4	22K	C4	22μ/16V
R5	1M	C5	0.022μ
R6	2.2M	C6	22μ/16V
R7	2.2M	C7	0.022μ
R8	330K	C8	100μ/16V
R9	620K	C9	100P
R10	270K	C10	3900P
R11	1M	C11	0.1μ
R12	100	C12	100μ/16V
R13	10K	C14	1000P

* All specs and applications shown above subject to change without prior notice.
(以上電路及規格僅供參考,本公司得逕行修正)