EE 560 CHIP INPUT AND OUTPUT (I/0) CIRCUITS

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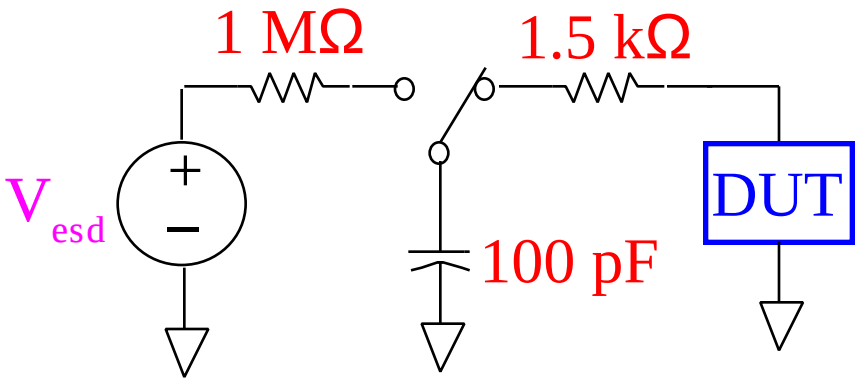
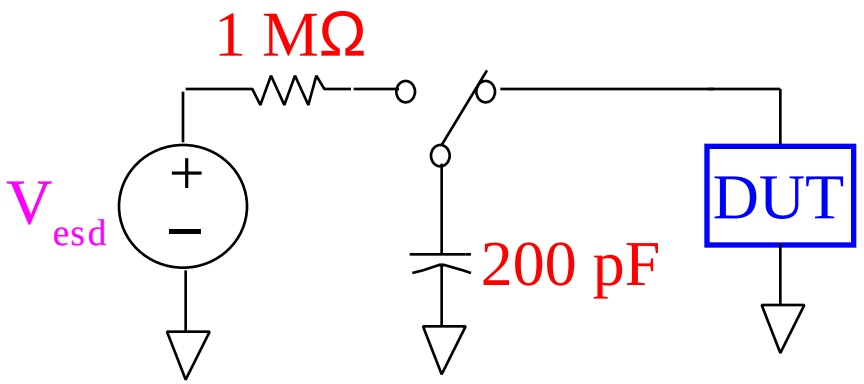
-> ESD PROTECTION CIRCUITS (INPUT PADS)
-> ON-CHIP CLOCK GENERATION & DISTRIBUTION
-> OUTPUT PADS
-> ON-CHIP NOISE DUE TO PARASITIC INDUCTANCE
-> SUPER BUFFER CIRCUIT DESIGN
-> LATCH-UP PHENOMENON

ESD PROTECTION

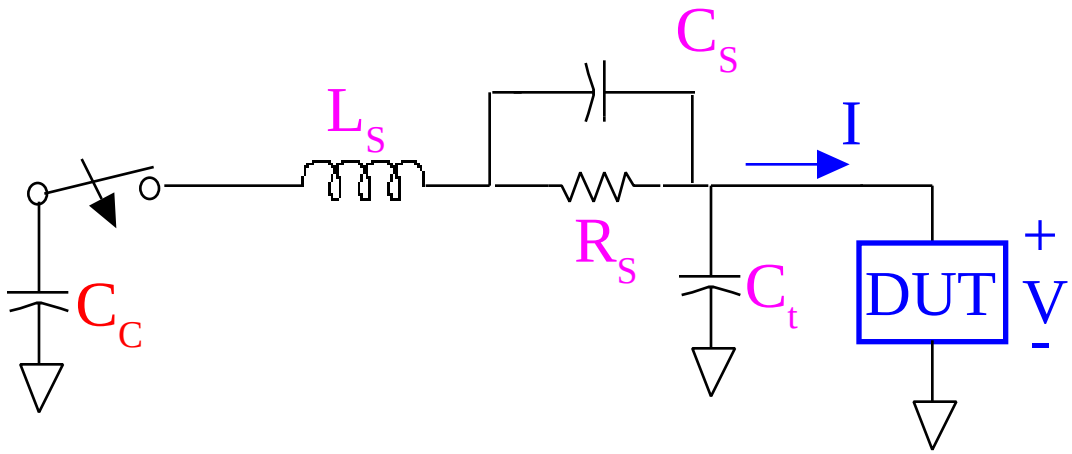
HUMAN BODY MODEL



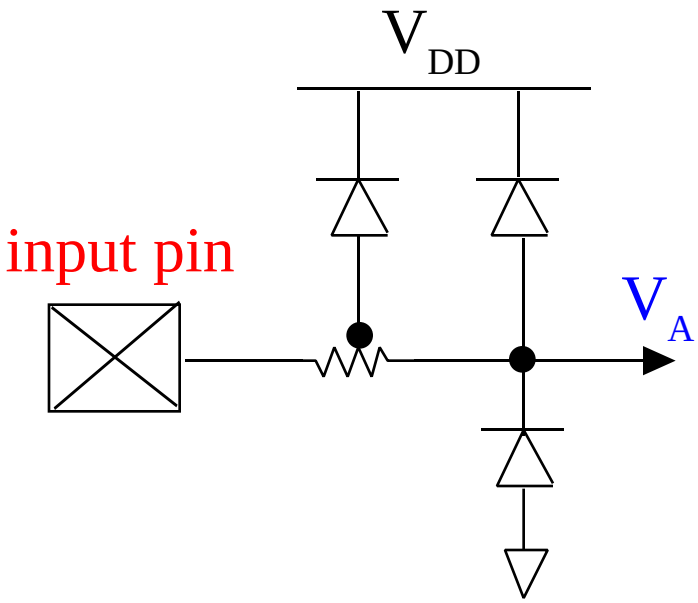
MACHINE MODEL



ESD TESTERS: LUMPED ELEMENT MODEL



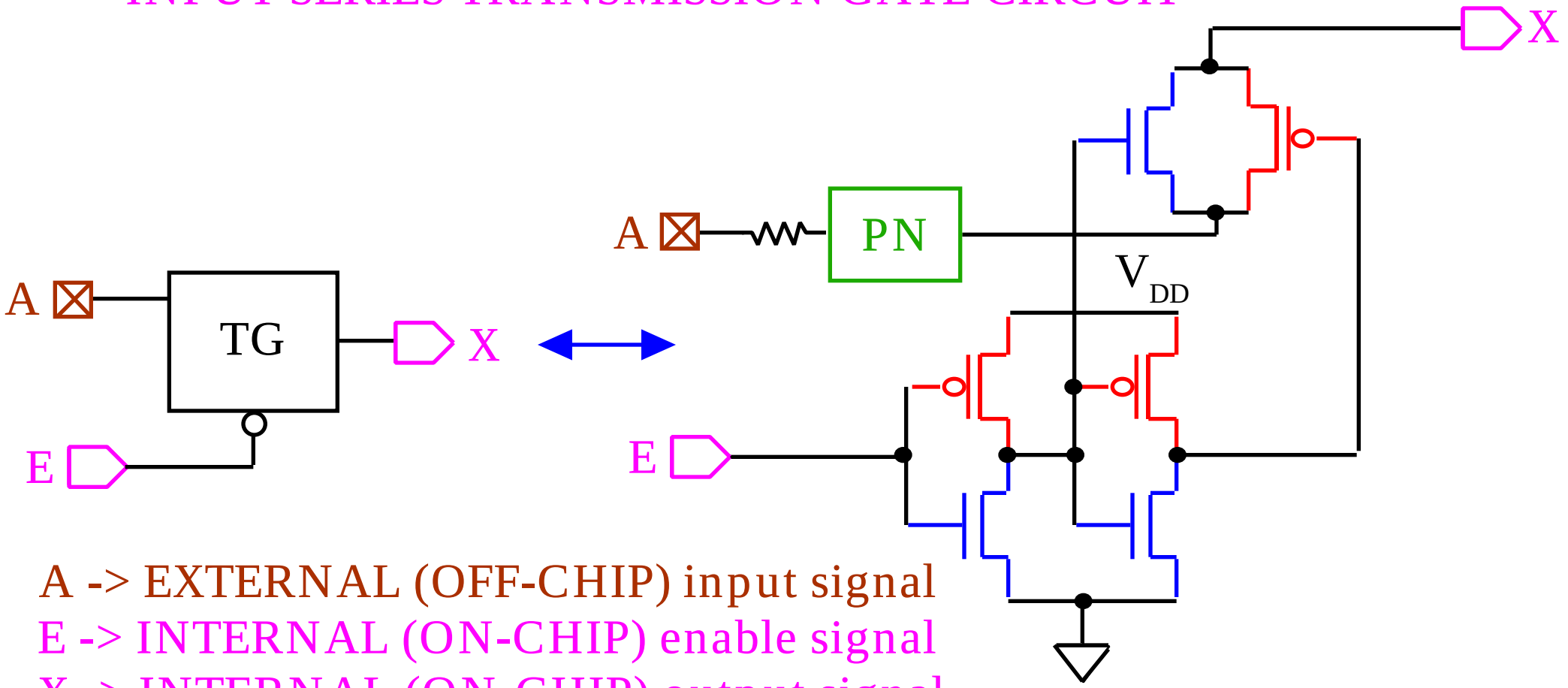
Component	HBM	MM
C_C (pF)	100	200
R_S (Ω)	1500	25
L_S (μH)	5	2.5
C_S (pF)	1	0
C_t (pF)	10	10



PROTECTION NETWORK (PN)

$$-0.7\ V < V_A < V_{DD} + 0.7\ V$$

INPUT SERIES TRANSMISSION GATE CIRCUIT

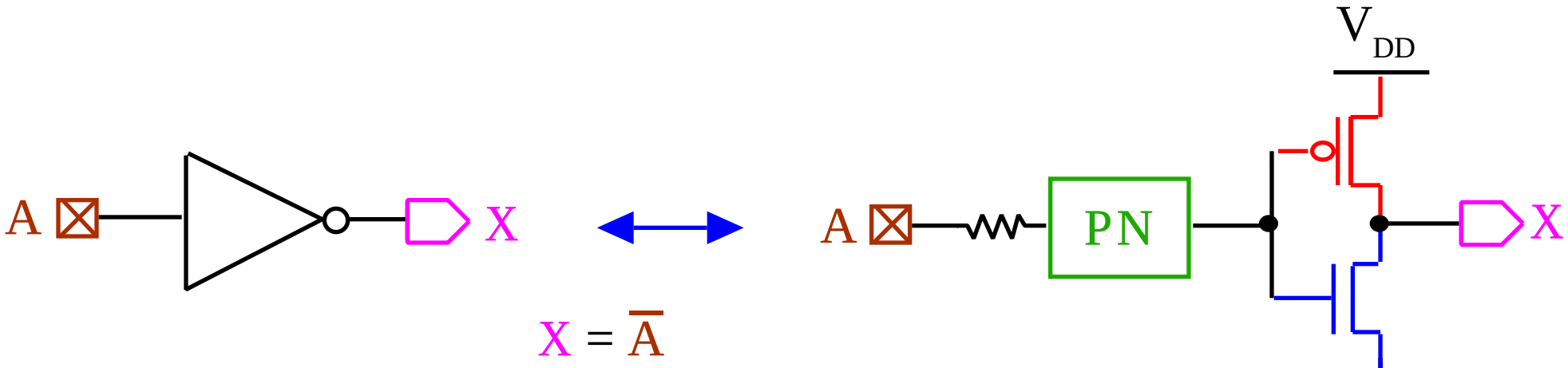


A -> EXTERNAL (OFF-CHIP) input signal
E -> INTERNAL (ON-CHIP) enable signal
X -> INTERNAL (ON-CHIP) output signal

X = A, when E = 0
X = HIGH-IMPEDANCE STATE when E = 1

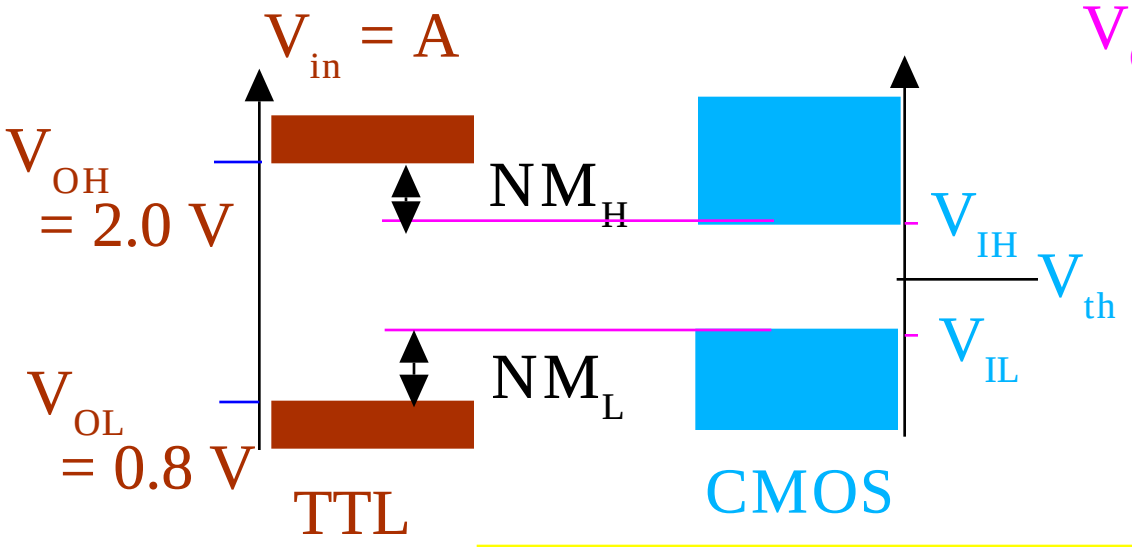
NOTE: ANY UNUSED INPUT TERMINALS SHOULD BE TIED TO V_{DD} OR GND USING PULL-UP OR PULL-DOWN RESISTORS RATHER THAN FLOAT

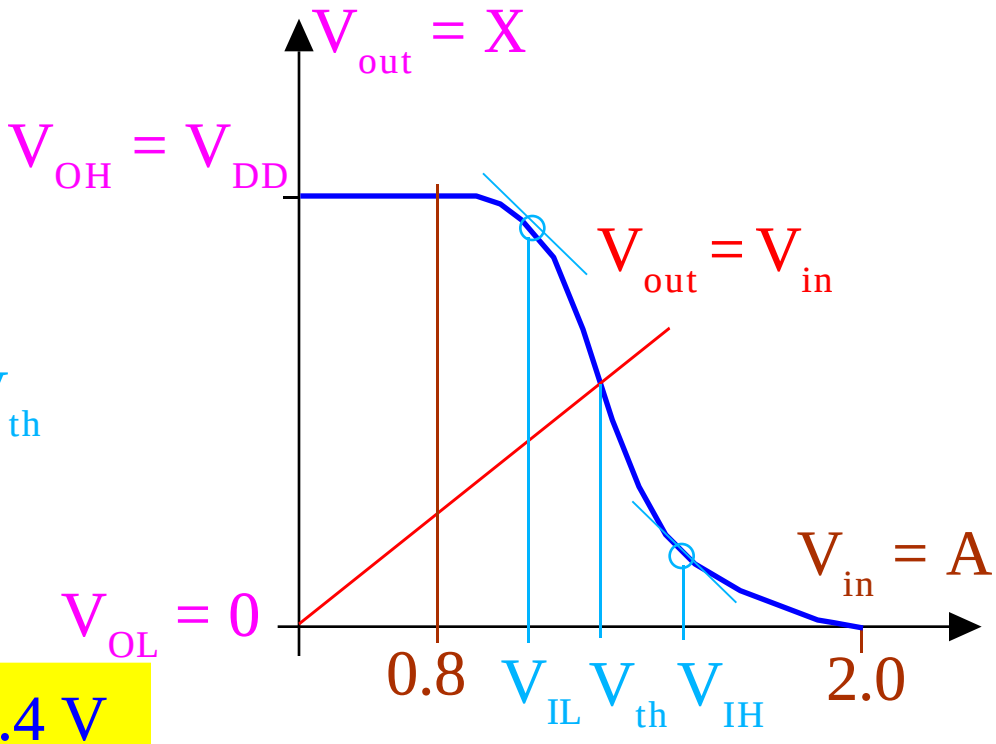
INVERTING INPUT CIRCUIT



$X = \overline{A}$

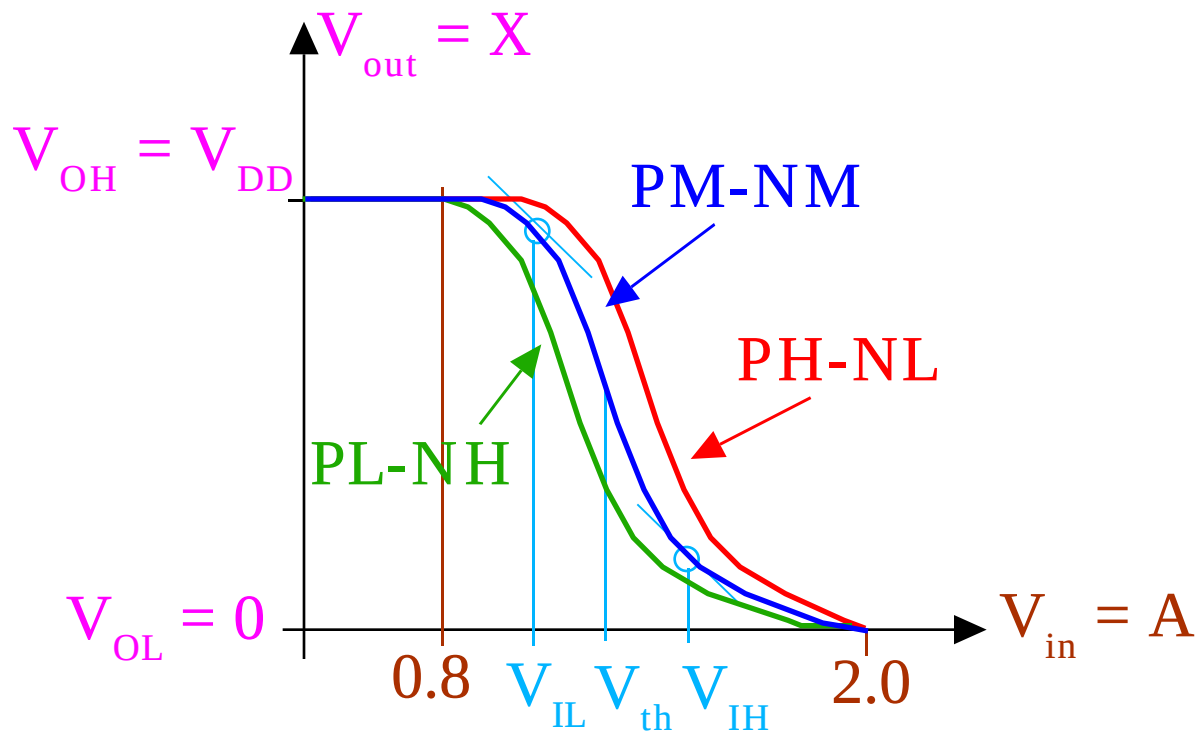
LEVEL SHIFTING FROM TTL TO CMOS





DESIGN FOR V_{th} = 1.4 V

VARIATIONS IN LEVEL SHIFT VTC DUE TO PRCESS VARIATIONS

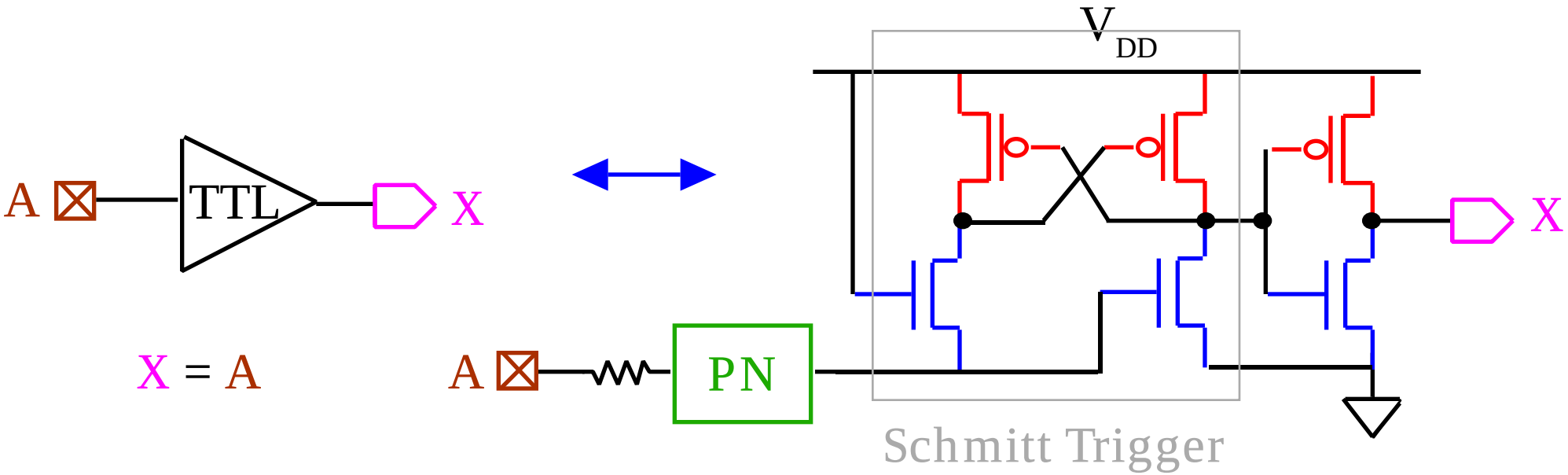


PM-NM => nominal processing

PH-NL => strong pMOS, weak nMOS process corner

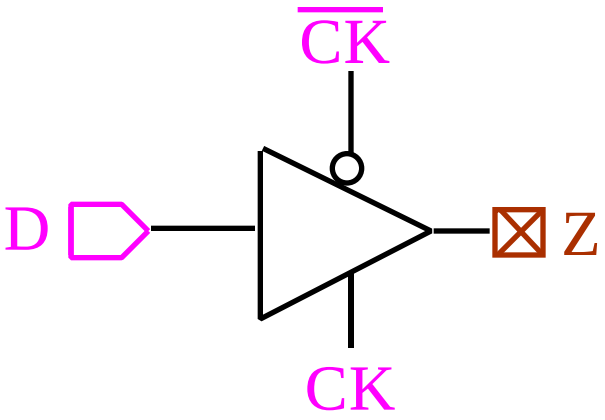
PL-NH => weak pMOS, strong nMOS process corner

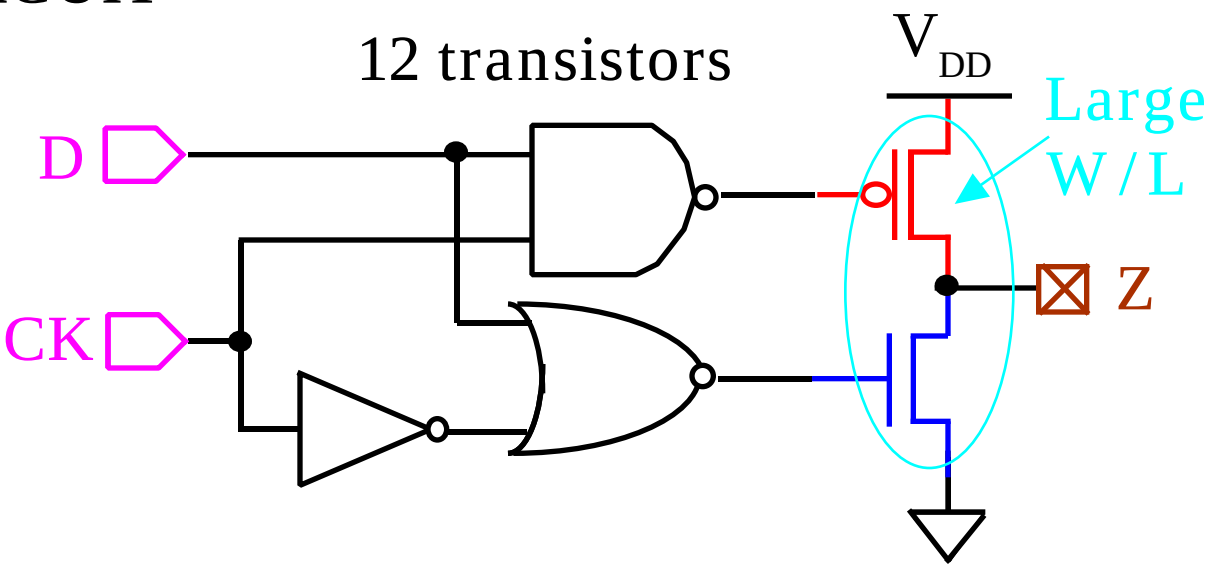
NON-INVERTING TTL LEVEL-SHIFTING CIRCUIT



OUTPUT CIRCUITS AND L(di/dt) NOISE

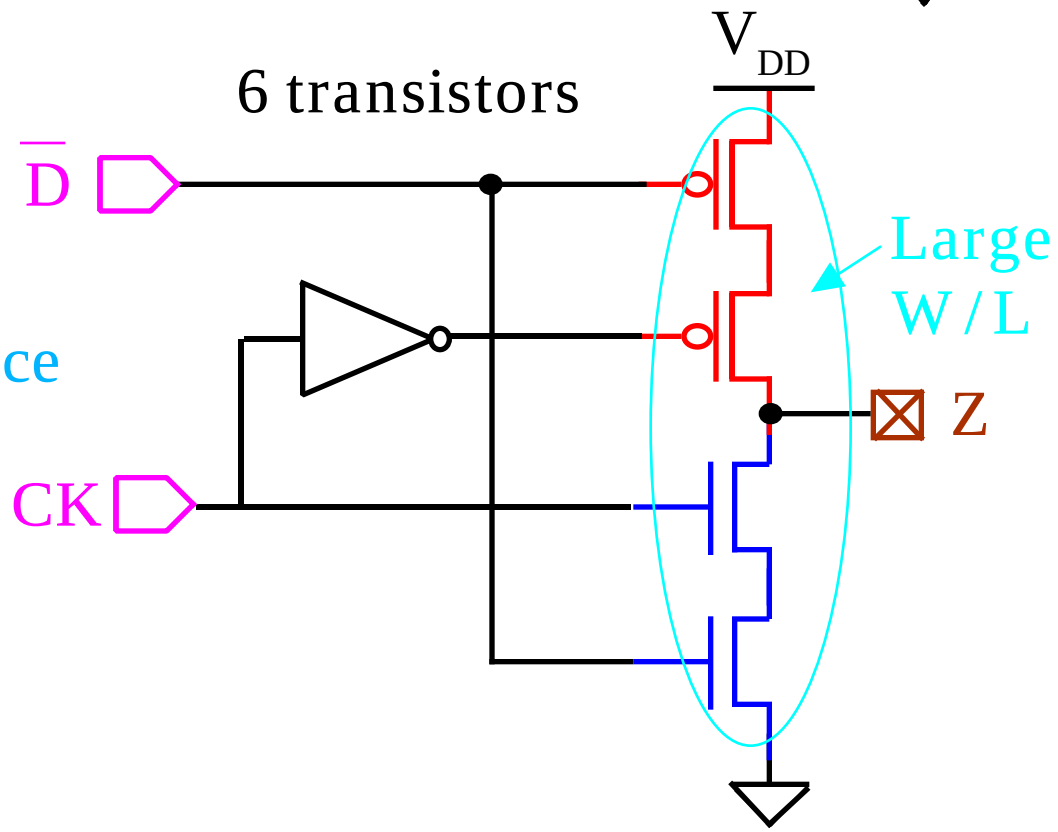
TRISTABLE OUTPUT CIRCUIT





Z = D for CK = 1
Z = HIGH IMP for CK = 0

LARGE W/L
-> Sufficent current sink, source
-> Reduce delay times



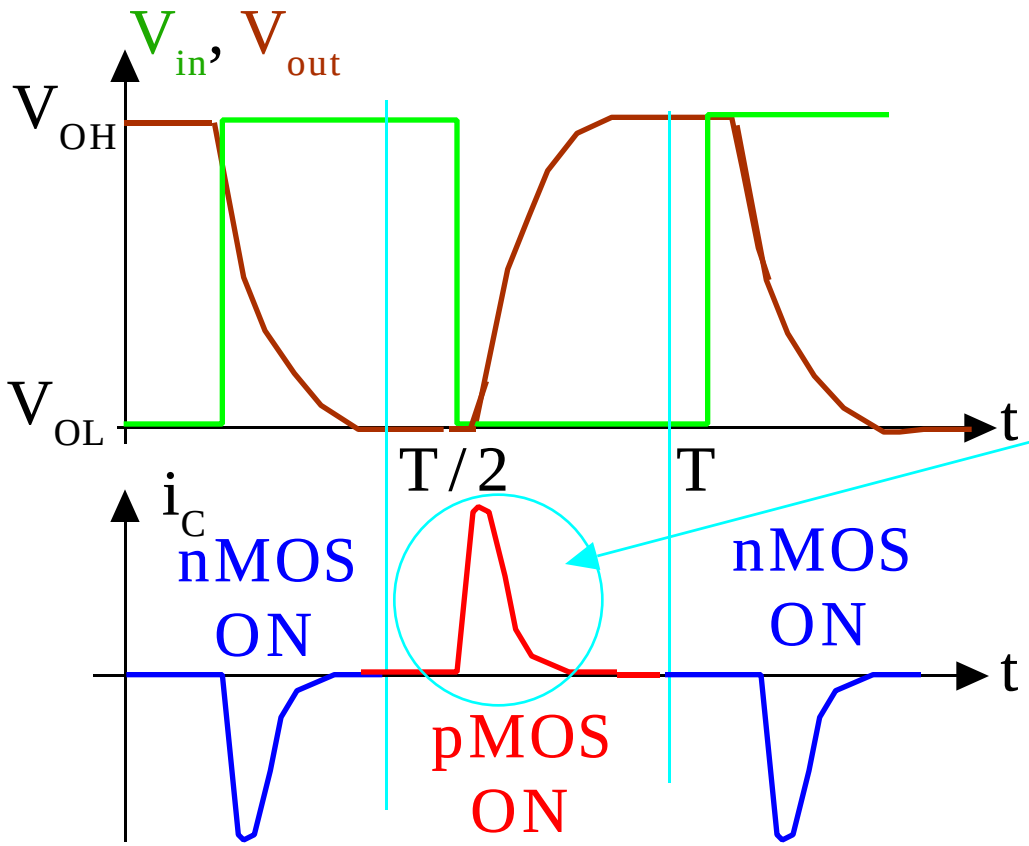
LARGE W / L

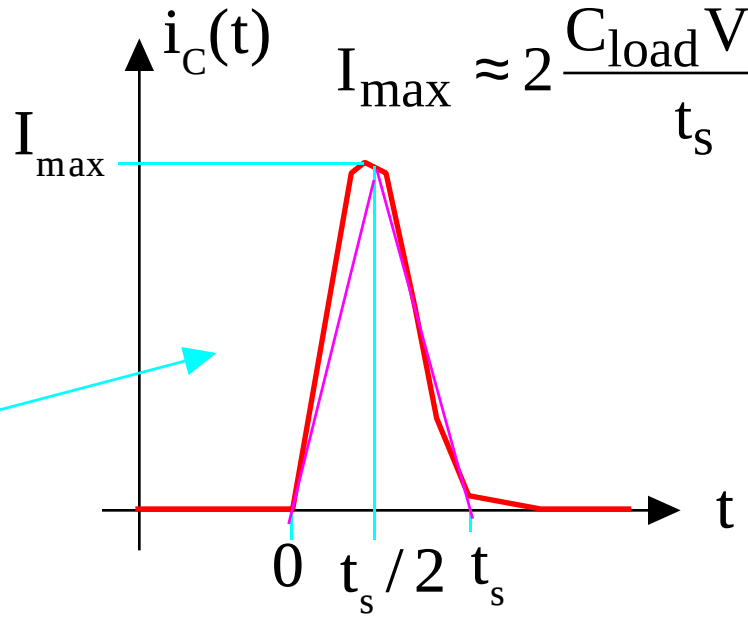
-> Sufficent current sink, source => LARGE di / dt

-> Reduce delay times

L (di / dt) VOLTAGE DROP ACROSS BONDING WIRE CONNECTING PAD TO PACKAGE PIN

$$I_{max}\frac{t_s}{2} \approx C_{load}V_{DD}$$





$$I_{max} \approx 2\frac{C_{load}V_{DD}}{t_s}$$

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{I_{max}}{t_s/2} = \frac{2I_{max}}{t_s}$$

$$\geq \frac{4C_{load}V_{DD}}{(t_s)^2}$$

$$\left(\frac{di}{dt}\right)_{max} \geq \frac{4\,C_{load}\,V_{DD}}{(t_s)^2}$$

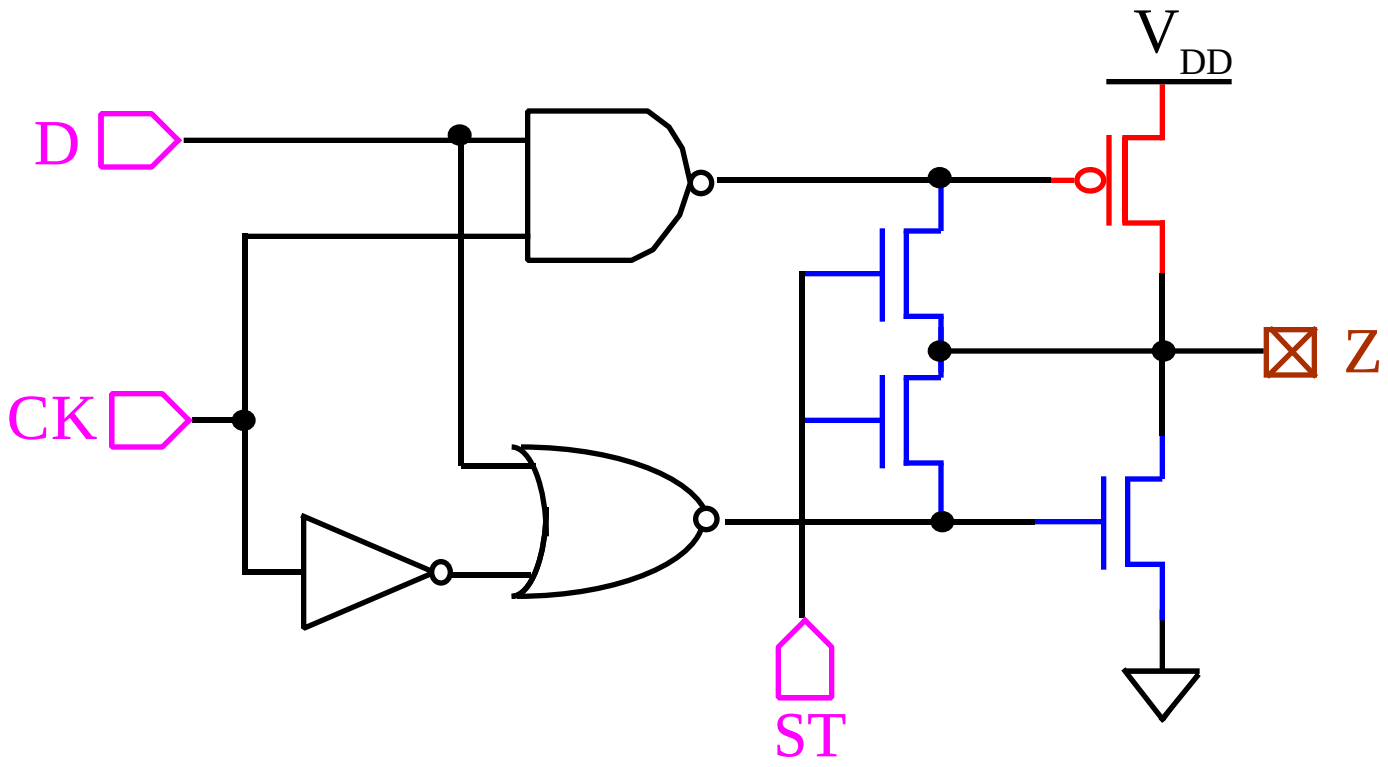
LET C_{load} = 100 pF, L = 2 nH, V_{DD} = 5 V and t_s = 5 ns

$$\left(\frac{di}{dt}\right)_{max} \geq \frac{4\left(100\,x10^{-12}\right)(5)}{\left(5\,x\,10^{-9}\right)^2} = 80\,\frac{mA}{ns}$$

$$L\left(\frac{di}{dt}\right)_{max} \geq 160\,mV$$

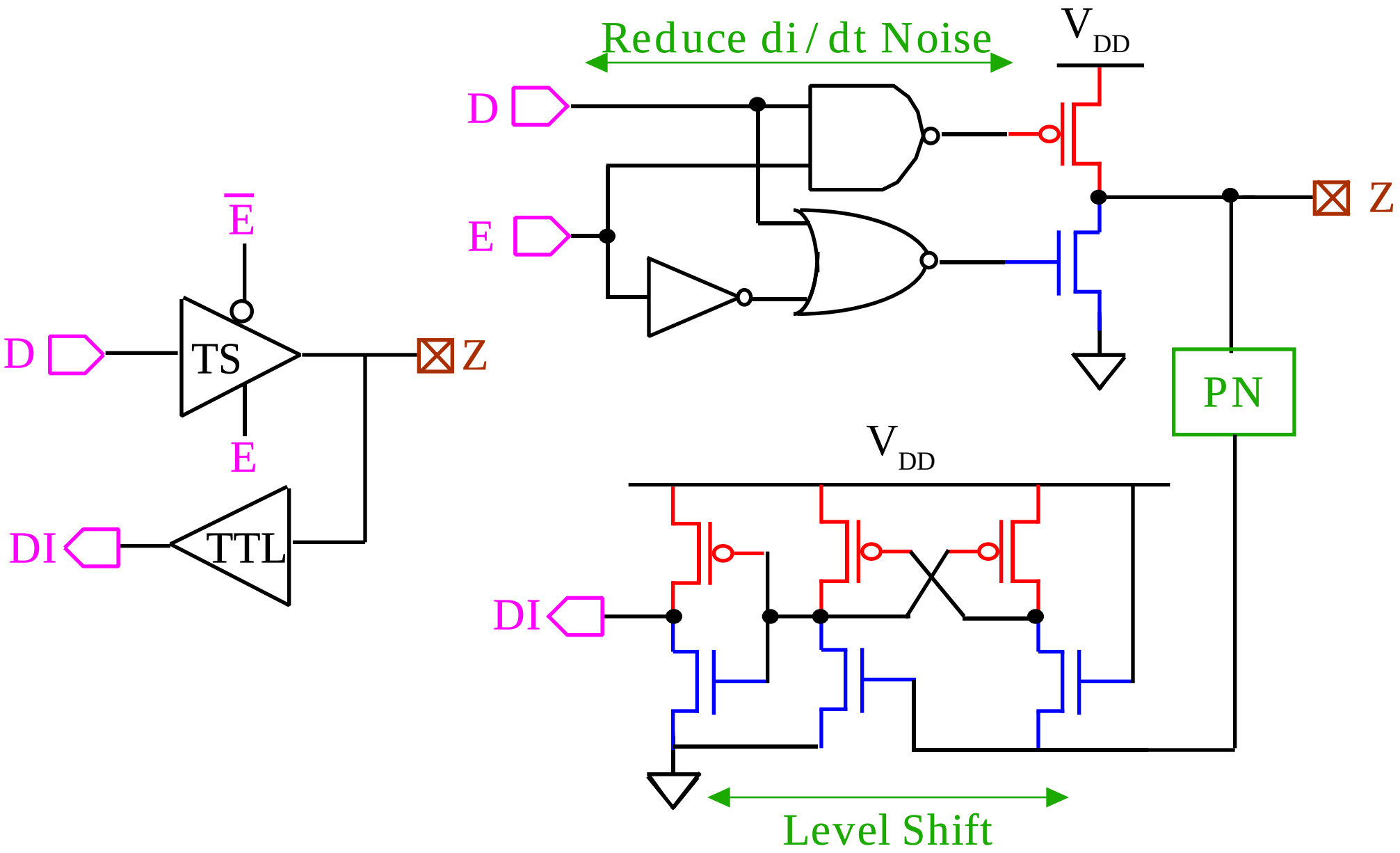
HIGH-END MICROPROCESSOR CHIPS WITH 32 BITS OR 64 BIT DATA BUS LINES - ALL OTPUT DRIVERS SWITCHING AT THE SAME TIME!

REDUCE L(di/dt) NOISE



PRECHARGES INVERTER OUTPUT "Z" TO $V_{DD}/2$ WHEN ST = 1 AND CK = 0 (JUST PRIOR TO CK -> 1)

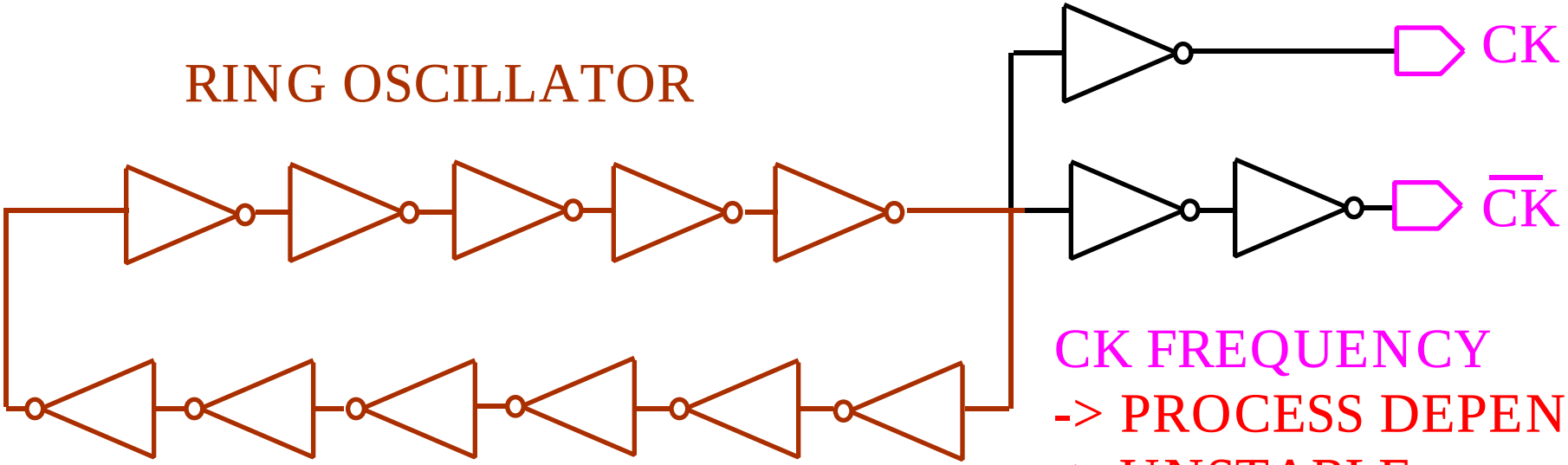
BIDRECTIONAL BUFFER CIRCUIT WITH TTL INPUT CAPABILITY



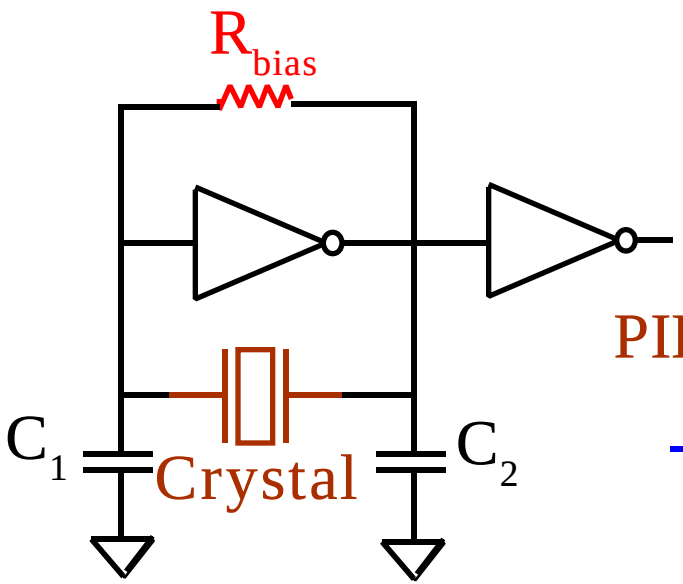
ON-CHIP CLOCK GENERATION AND DISTRIBUTION

SIMPLE ON-CHIP CLOCK CIRCUIT

RING OSCILLATOR



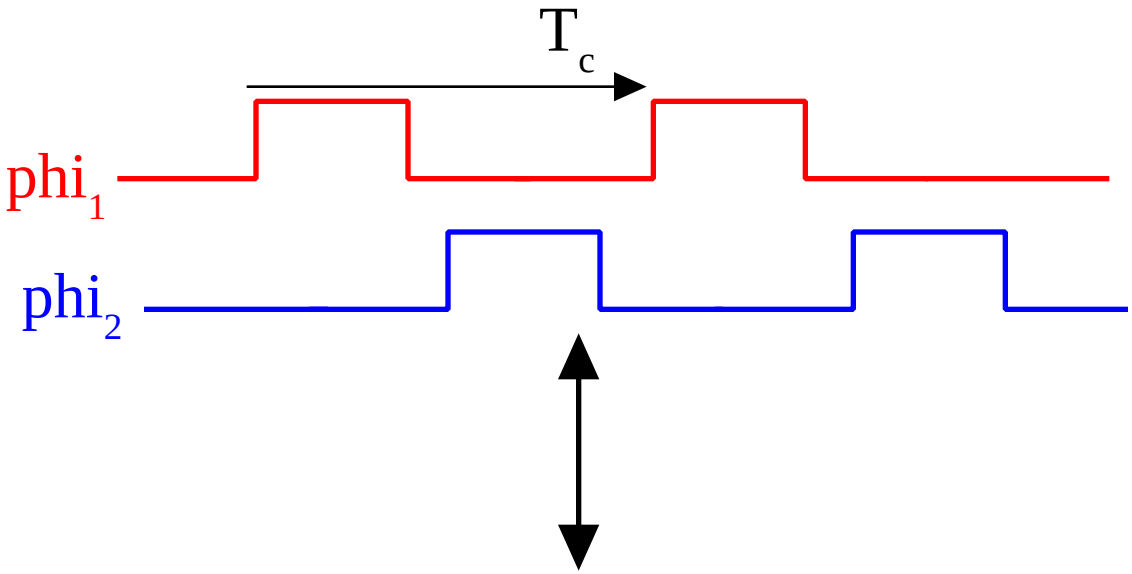
CK FREQUENCY
-> PROCESS DEPENDENT
-> UNSTABLE

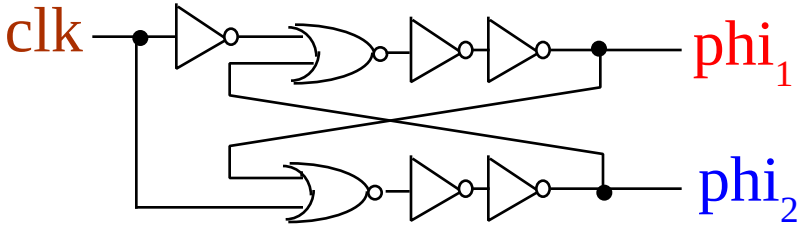


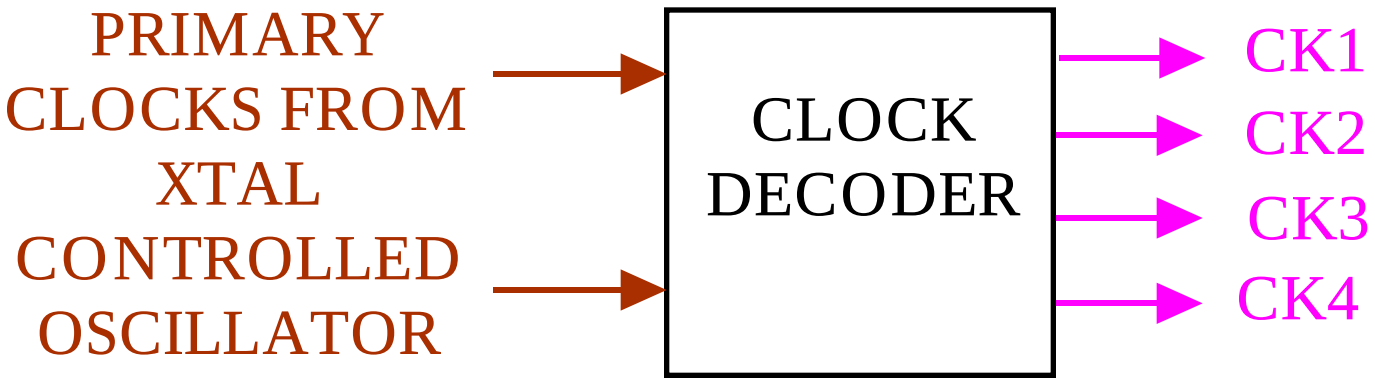
PIERCE CRYSTAL OSCILLATOR CIRCUIT

-> GOOD FREQUENCY STABILITY

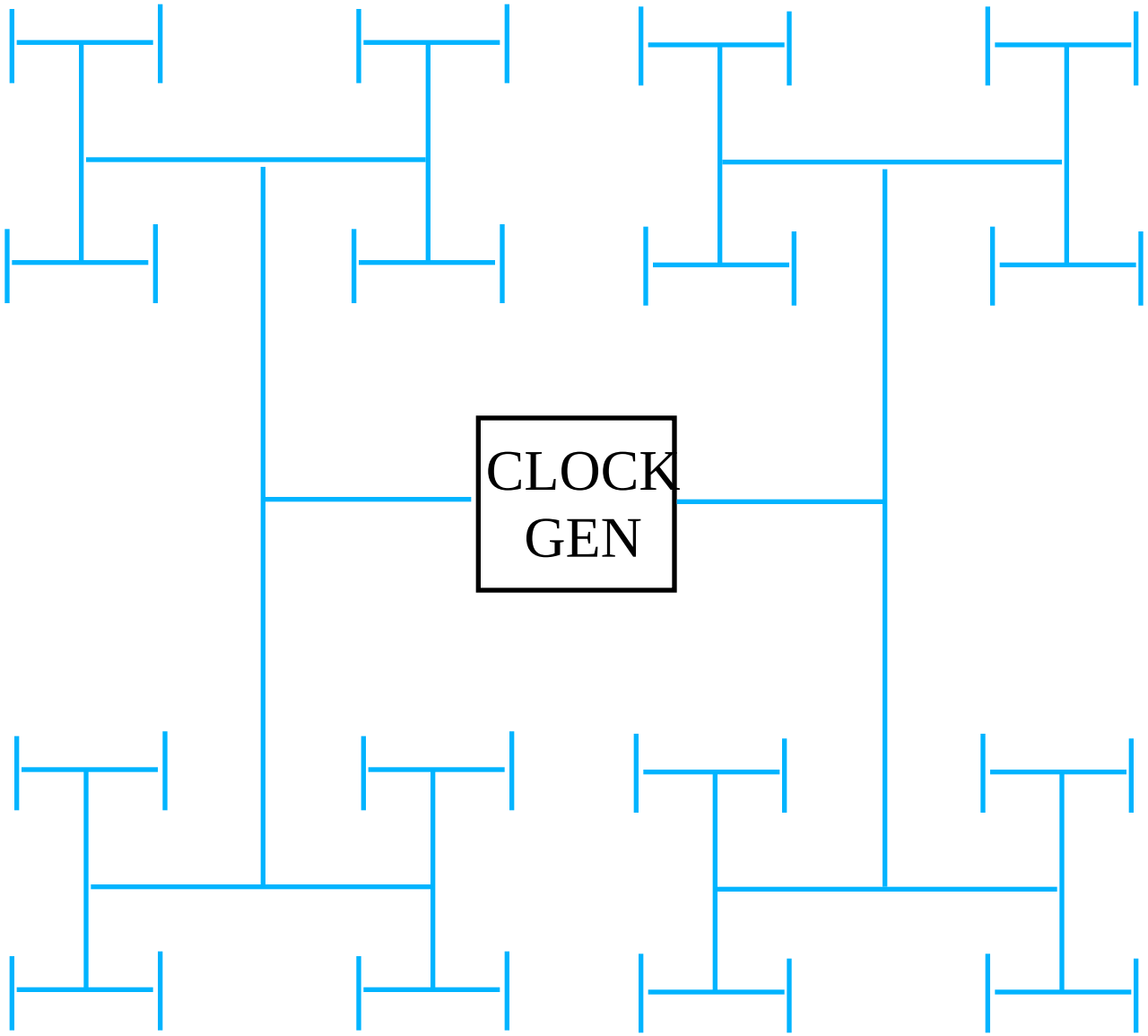
TWO-PHASE CLOCKING SCHEMES



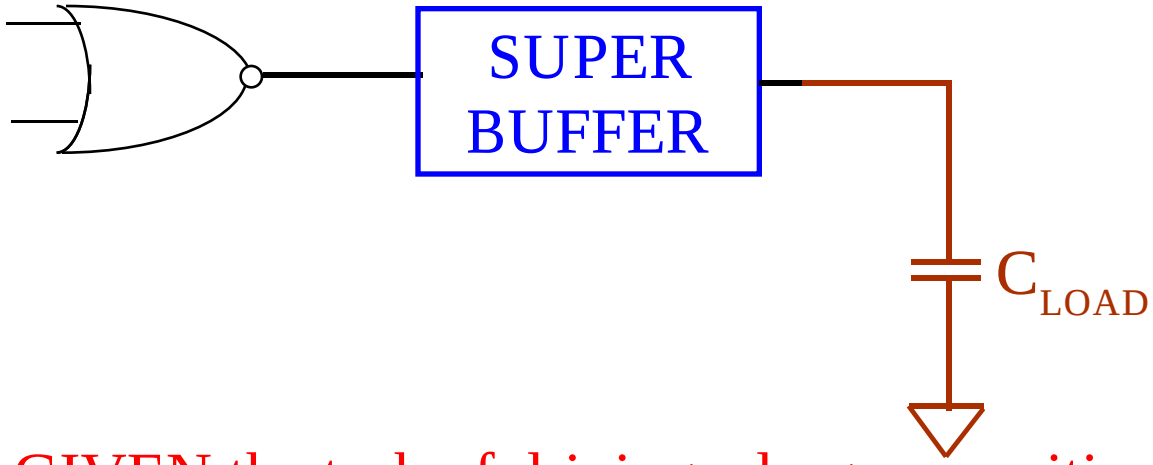




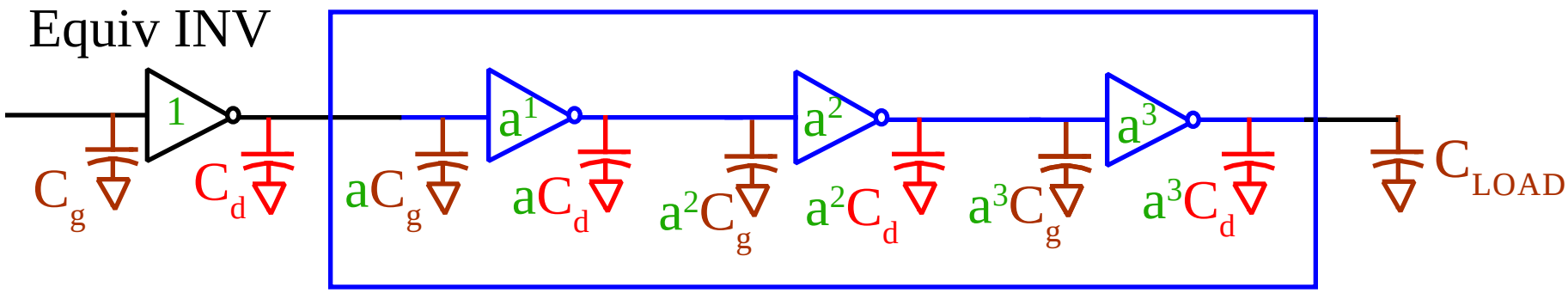
GENERAL LAYOUT OF H-TREE CLOCK DISTRIBUTION NETWORK FOR UNIFORM CLOCK DISTRIBUTION



C AD Techniques to automate the generation of optimum clock distribution networks.



PROBLEM: GIVEN the task of driving a large capacitive load C_{LOAD}, how can a SUPER BUFFER comprised of chain of N inverters be scaled to minimize the buffer's delay time?



N = 3

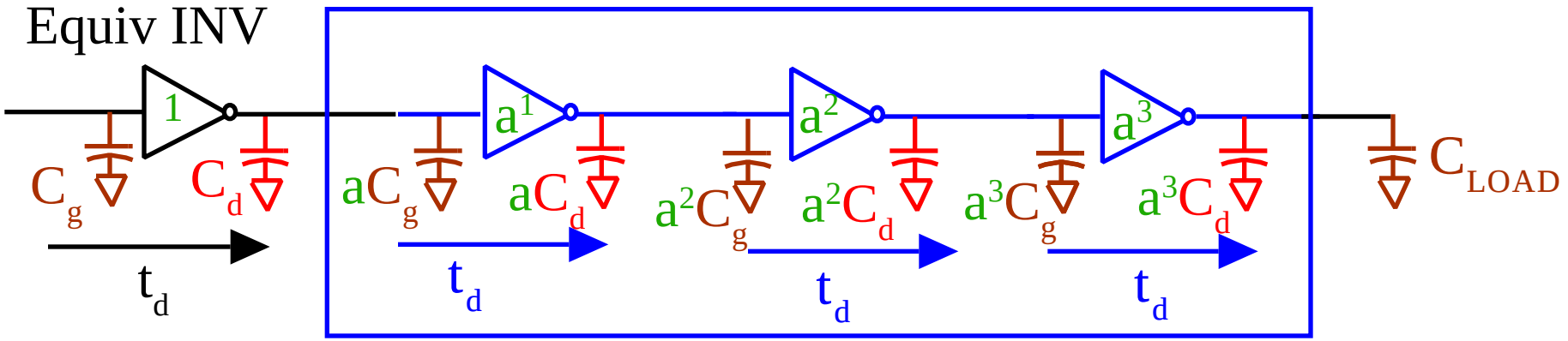
let $C_{LOAD} = a^4 C_g$

N -> number of inverter stages

a -> optimal stage scale factor

In General:

$C_{LOAD} = a^{N+1} C_g$



N = 3

let $C_{LOAD} = a^4 C_g$

N -> number of inverter stages

a -> optimal stage scale factor

In General:

$C_{LOAD} = a^{N+1} C_g$

CONSIDER N stages and $C_{LOAD} = a^{N+1} C_g$

ALL INVERTERS HAVE SAME DELAY

$$t_d = \tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

τ_0 is per gate delay for Equiv INV in ring oscillator circuit with load capacitance = $C_g + C_d$.

$$t_{total} = (N+1)\tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

Choose N and a to MINIMIZE t_{total}

where $C_{LOAD} = a^{N+1} C_g$ =>

$$N+1 = \frac{\ln\left(C_{LOAD}/C_g\right)}{\ln(a)}$$

$$t_{total} = (N+1)\tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

$$N+1 = \frac{\ln\left(C_{LOAD}/C_g\right)}{\ln(a)}$$

$$\Rightarrow \quad t_{total} = \frac{\ln\left(C_{LOAD}/C_g\right)}{\ln(a)} \tau_0 \frac{C_d + aC_g}{C_d + C_g}$$

TO MINIMIZE t_{total}:

$$\frac{dt_{total}}{da} = \tau_0 \ln\left(\frac{C_{LOAD}}{C_g}\right) \underbrace{\left[-\frac{1/a}{(\ln(a))^2} \left(\frac{C_d + aC_g}{C_d + C_g}\right) + \frac{1}{\ln(a)} \left(\frac{C_g}{C_d + C_g}\right) \right]}_{= 0} = 0$$

$$a_{opt}\left[\ln\left(a_{opt}\right) - 1\right] = \frac{C_d}{C_g}$$

For the SPECIAL CASE $C_d = 0$ => $\ln(a_{opt}) = 1$ or $a_{opt} = e^1 = 2.718$

EXAMPLE: For C_d = 0.5 fF, C_g = 10 fF, determine a_{opt} and N for C_{LOAD} = 50 pF.

$$a_{opt}\,[\ln(a_{opt}) - 1] = 0.5 \Rightarrow a_{opt} = 3.18$$

$$N+1 = \frac{\ln\left(C_{LOAD}/C_g\right)}{\ln(a)}$$

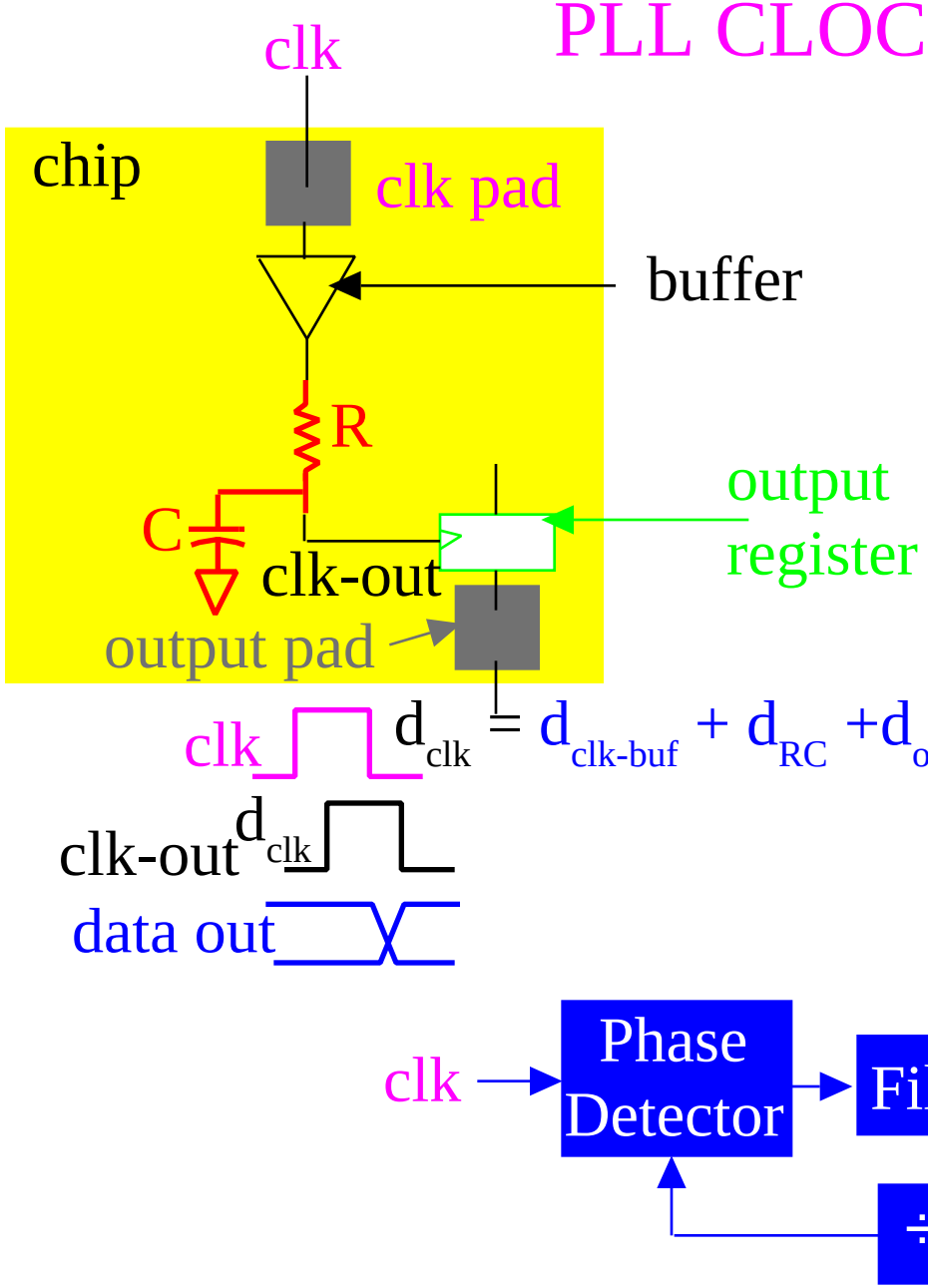
$$N = [\ln(C_{LOAD}/C_g)/\ln(a)] - 1$$
$$= [\ln(50 \times 10^{-12}/1 \times 10^{-14})/\ln(3.18)] - 1$$
$$= [\ln(5000)/\ln(3.18)] - 1 = 6.36$$

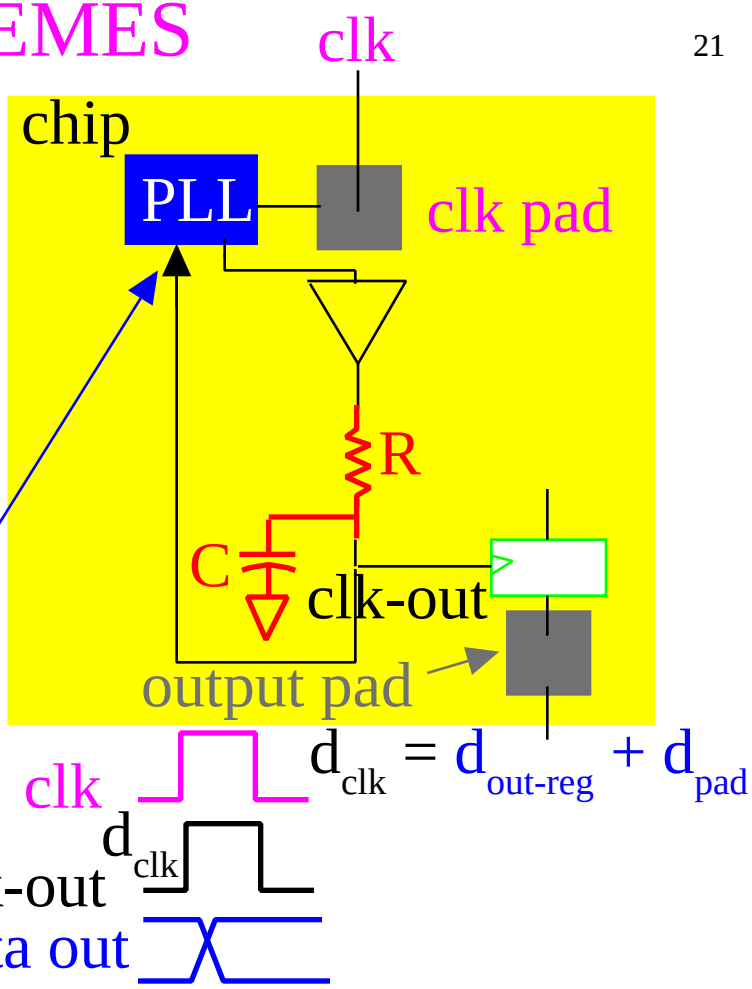
The SUPER BUFFER DESIGN which MINIMIZES t_{total} for C_{LOAD} = 50 pF is

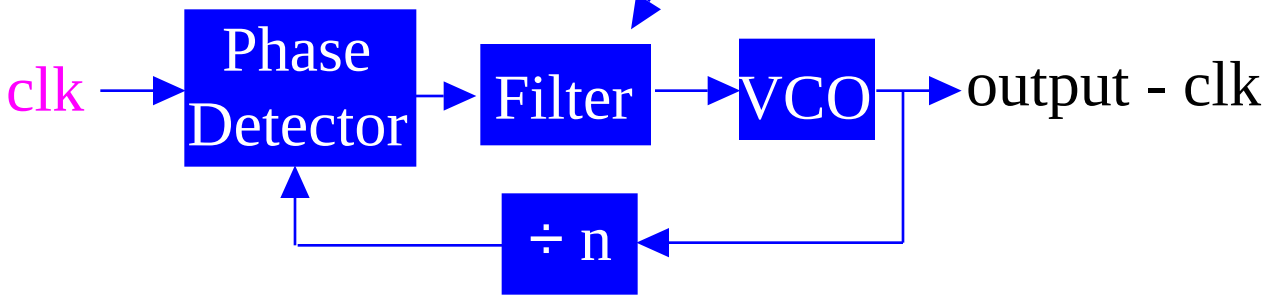
N = 7 Equiv INV stages

a_{opt} = 3.18

PLL CLOCKING SCHEMES



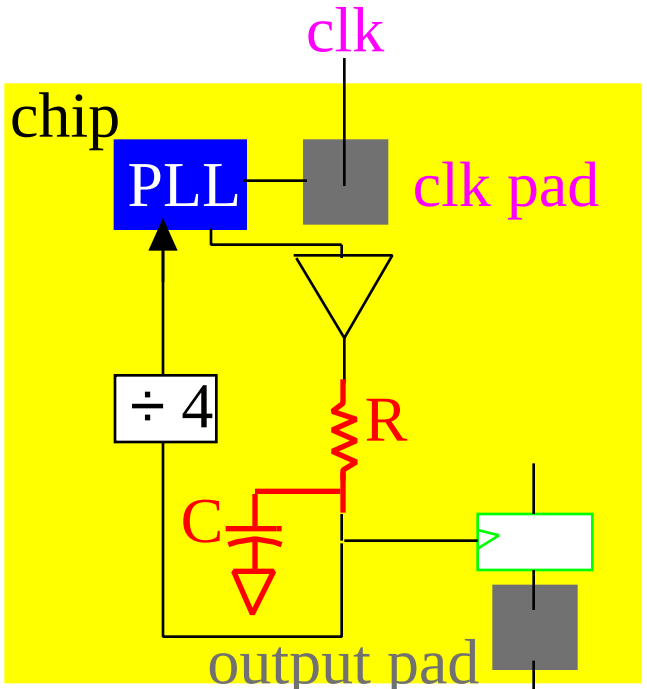




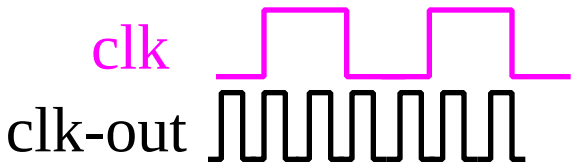
WHY USE PLL IN SYSTEM CLOCKS?

+ To syncronize the internal clock of a chip to an external clock.

+ To operate an internal clock at a higher rate than the external clock input.

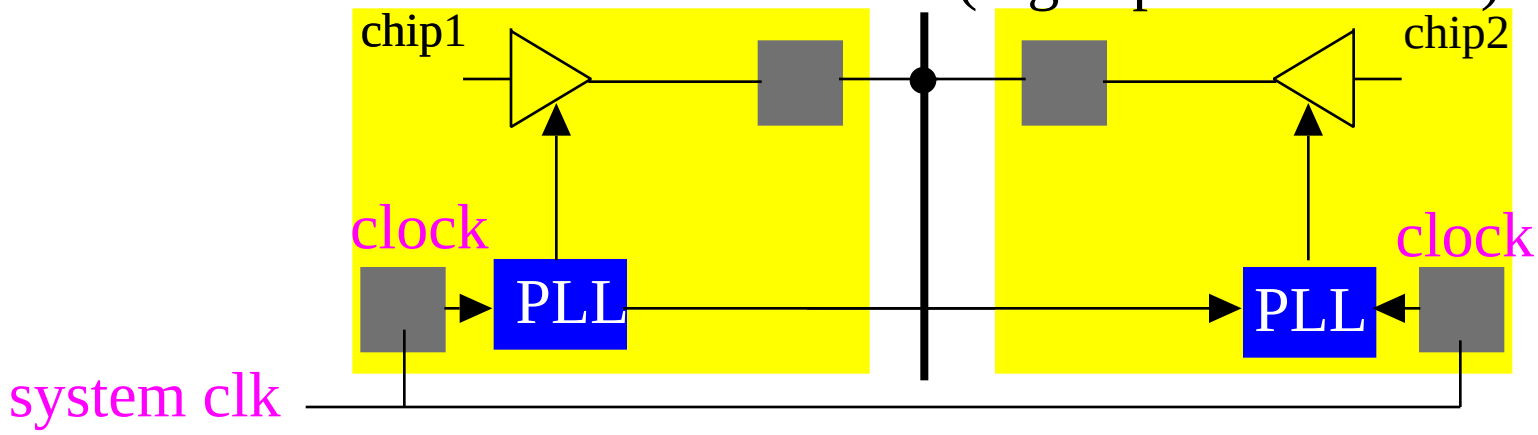


Generates an internal
fclk-out = 4 × fclk
synchronized to clk



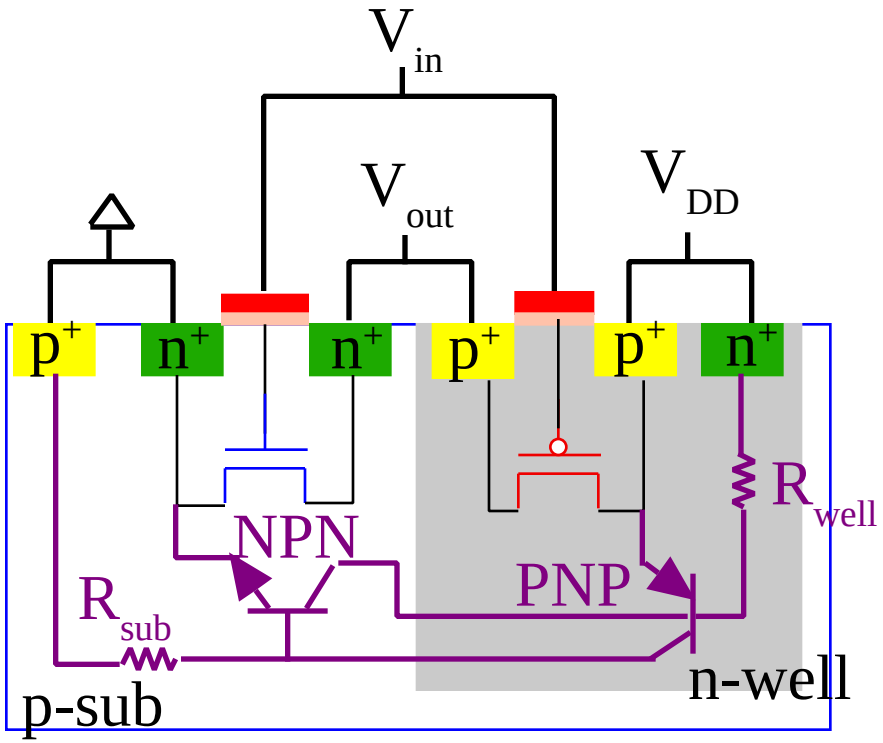
$d_{clk} = d_{out\text{-}reg} + d_{pad}$

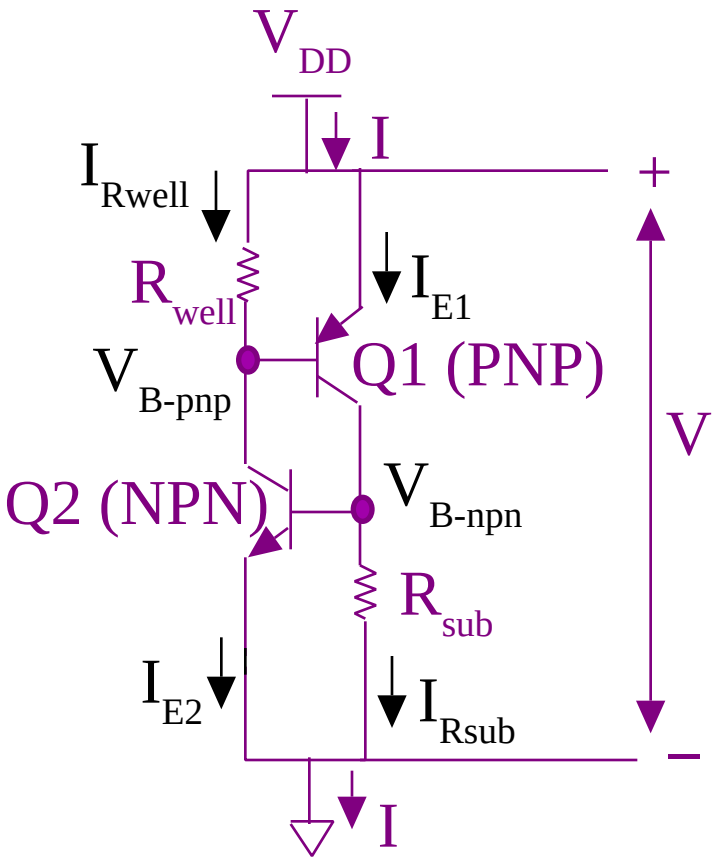
sychronizes the out-put enables of two chips
bus (high speed - tristate)

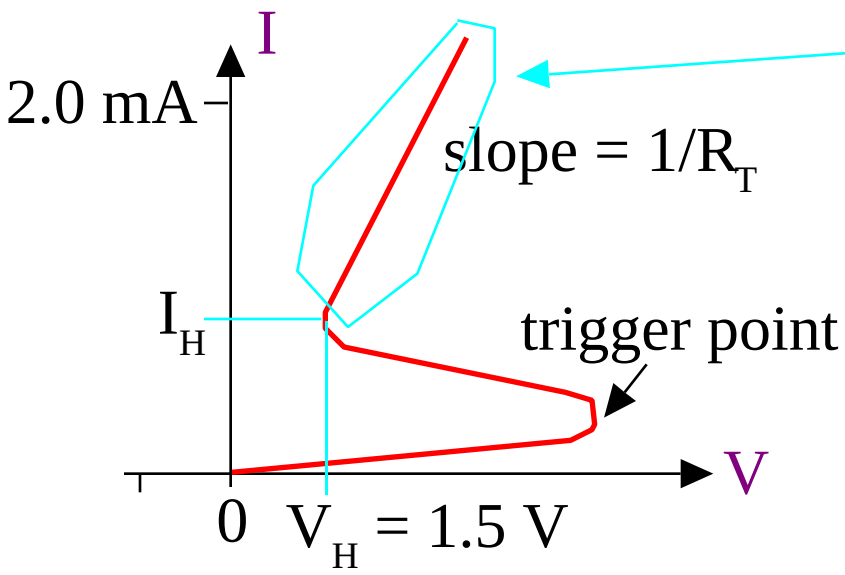


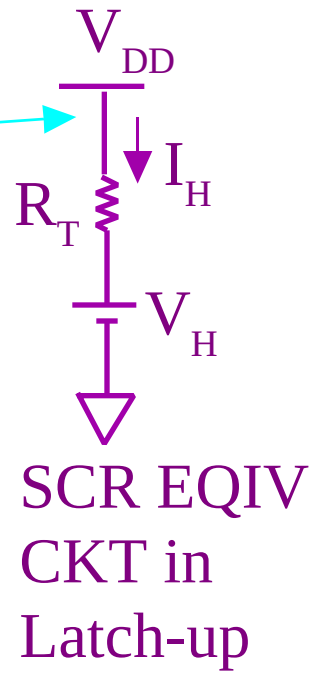
LATCHUP IN CMOS CIRCUITS

latch-up susceptability
α 1/[NSUB (spacing)^2]

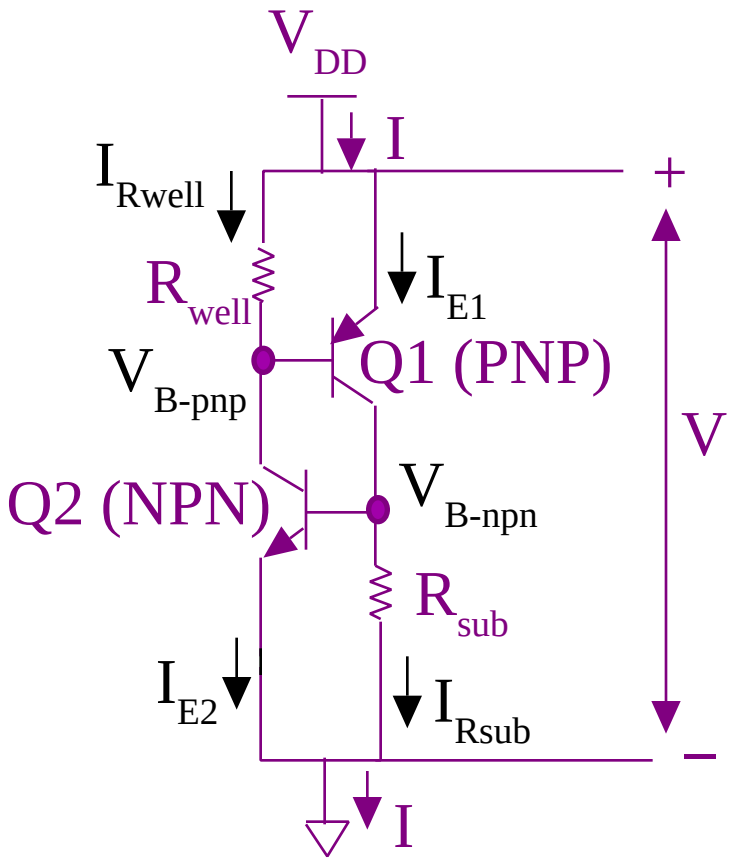


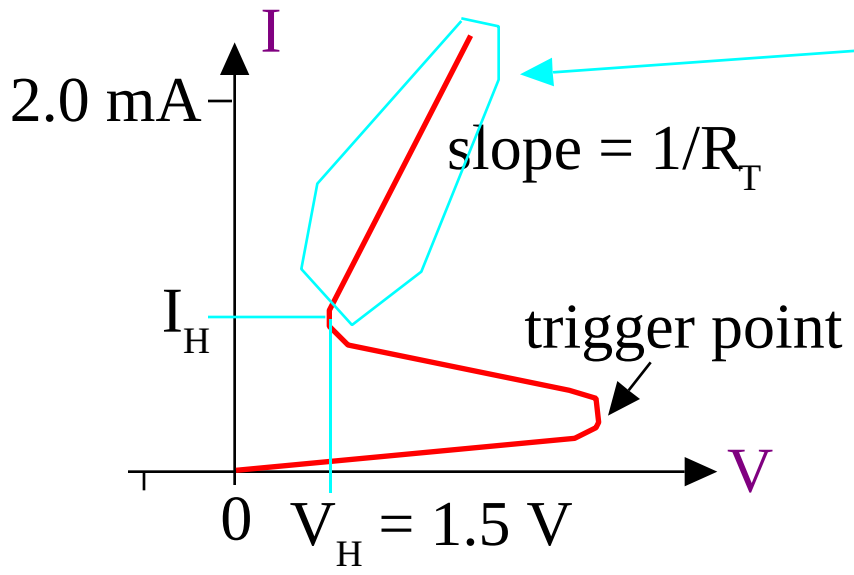


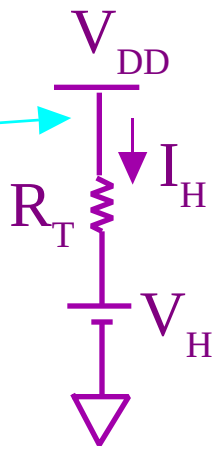




SCR EQIV CKT in Latch-up







SCR EQIV CKT in Latch-up

$$I_H = \frac{I_{Rsub}\alpha_{pnp} + I_{Rwell}\alpha_{npn}}{\alpha_{pnp} + \alpha_{npn} - 1}$$

At the on-set of latch-up

$I > I_H = (V_{DD} - V_H)/R_T$

LATCH-UP CONDITION

$$\alpha_{npn} + \alpha_{pnp} \geq 1 + \left(\frac{\frac{R_T}{R_{well}}\alpha_{pnp} + \frac{R_T}{R_{sub}}\alpha_{npn}}{\frac{V_{DD}}{V_{BE-sat}} - 2} \right)$$

LATCH-UP PREVENTION

make large

$$\alpha_{npn} + \alpha_{pnp} \geq 1 + \left(\frac{\frac{R_T}{R_{well}}\alpha_{pnp} + \frac{R_T}{R_{sub}}\alpha_{npn}}{\frac{V_{DD}}{V_{BE-sat}} - 2} \right)$$

make small

Reduce α_{npn}, α_{pnp}; Reduce R_{sub}, R_{well}

Latchup Prevention LAYOUT Guidelines:

A. Latchup resistant CMOS processes (thin epi layer on highly doped substrate).

B. Layout n and p channel transistors such that all nMOS transistors are placed close to GND and V_{DD}. Physically separate n and p transistors (i.e. with the bonding pad).

C. Use p^+ guard rings connected to GND around nMOS transistors and n^+quard rings connected to V_{DD} around the pMOS transistors to reduce R_{well} and R_{sub} and to weaken BJTs.

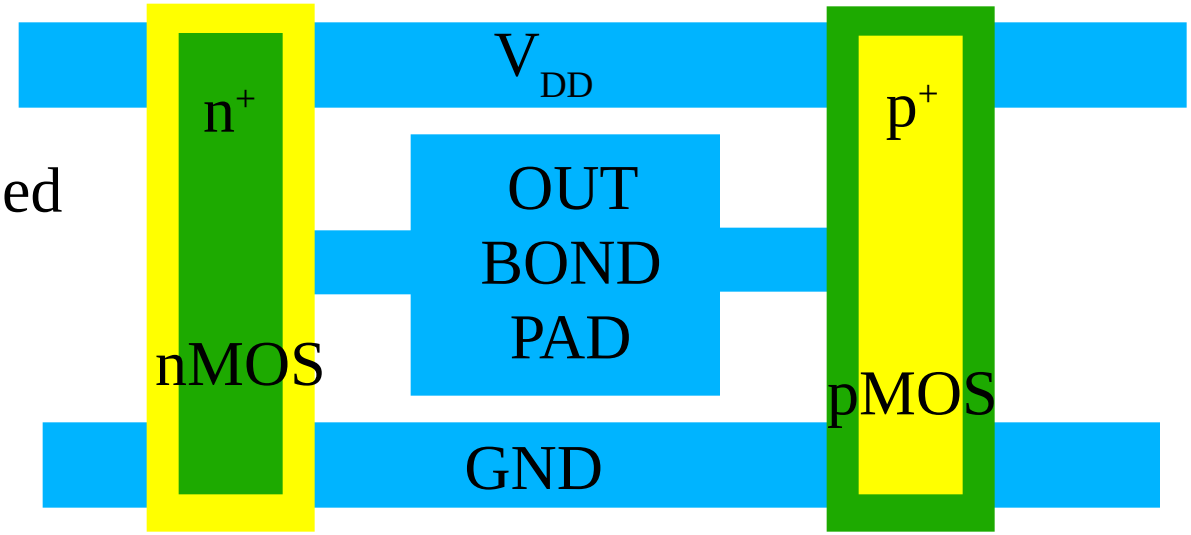
D. Place sub, well contacts close to the nMOS, pMOS source connections to supply rails (i.e. GND for nMOS, V_{DD} for pMOS).

CONSERVATIVE RULE: One sub contact per source connection to a supply

LESS CONSERVATIVE: One sub contact per 5-10 devices.

I/O CELL LAYOUT USING LATCH-UP GUIDELINES

p-tub edge spaced far from p^+ sources to V_{DD}



p^+ guard ring to GND

n^+ guard ring to V_{DD}