EE 560 MOS INVERTERS: DYNAMIC CHARACTERISTICS

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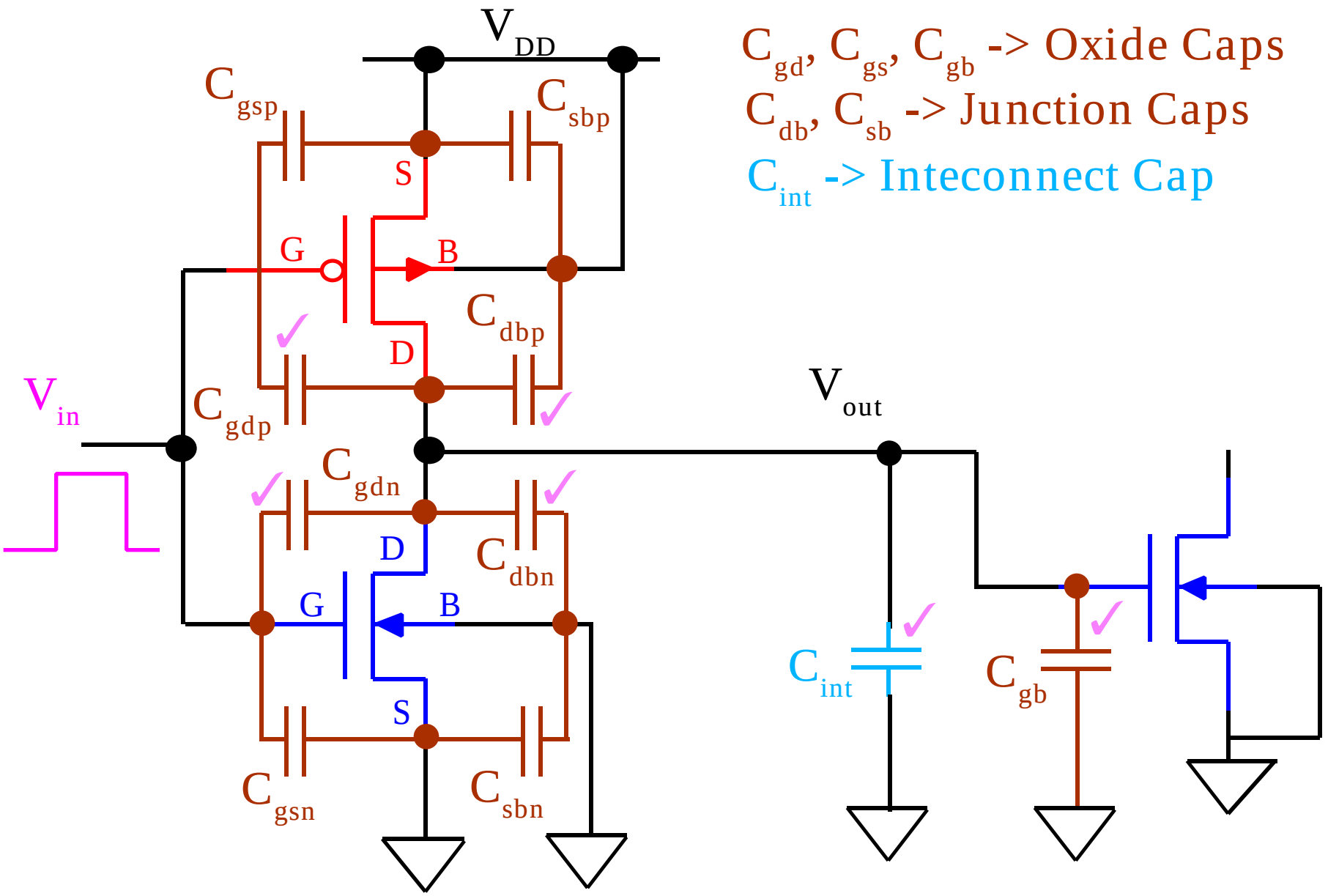
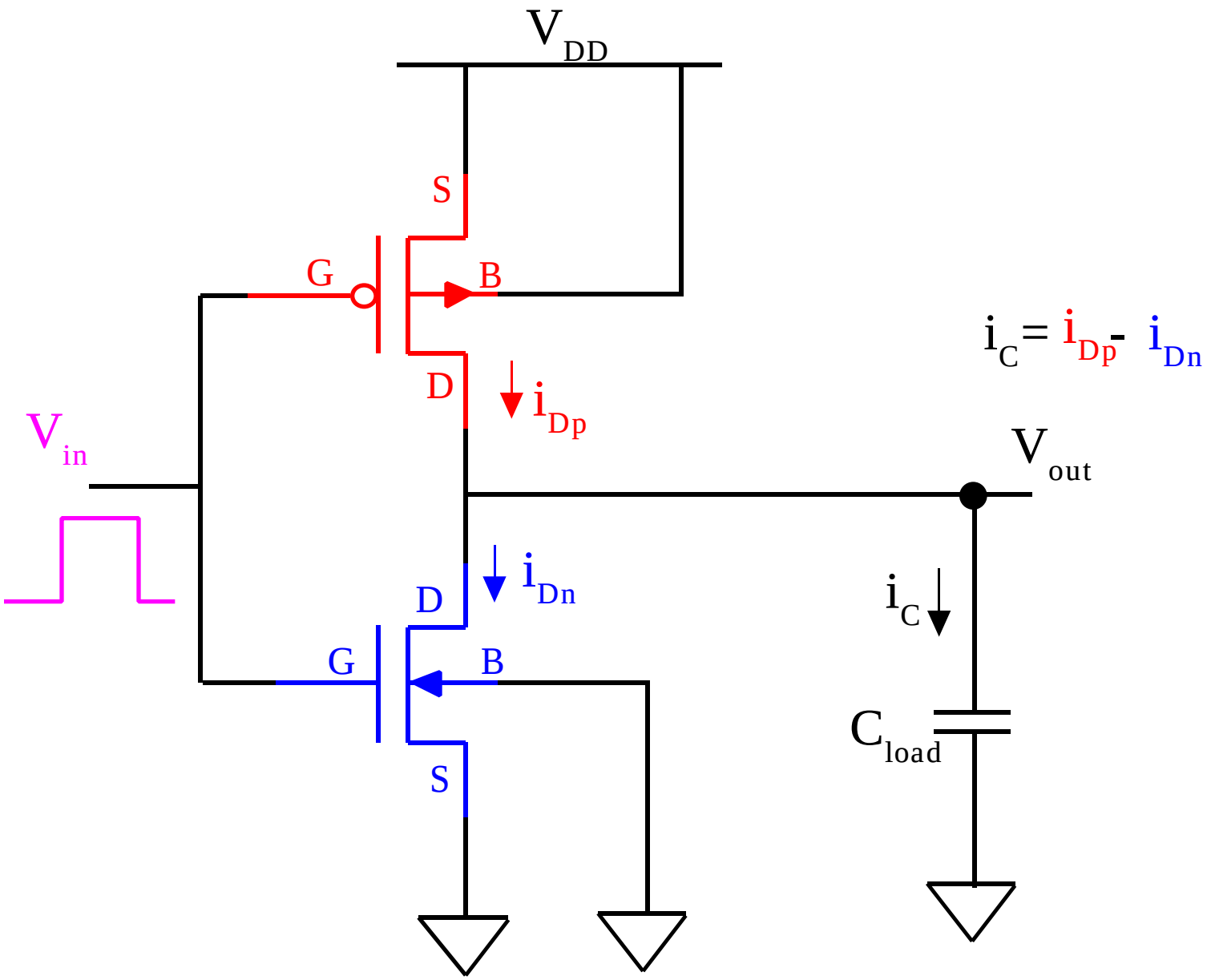


C_{gd}, C_{gs}, C_{gb} -> Oxide Caps

C_{db}, C_{sb} -> Junction Caps

C_{int} -> Inteconnect Cap

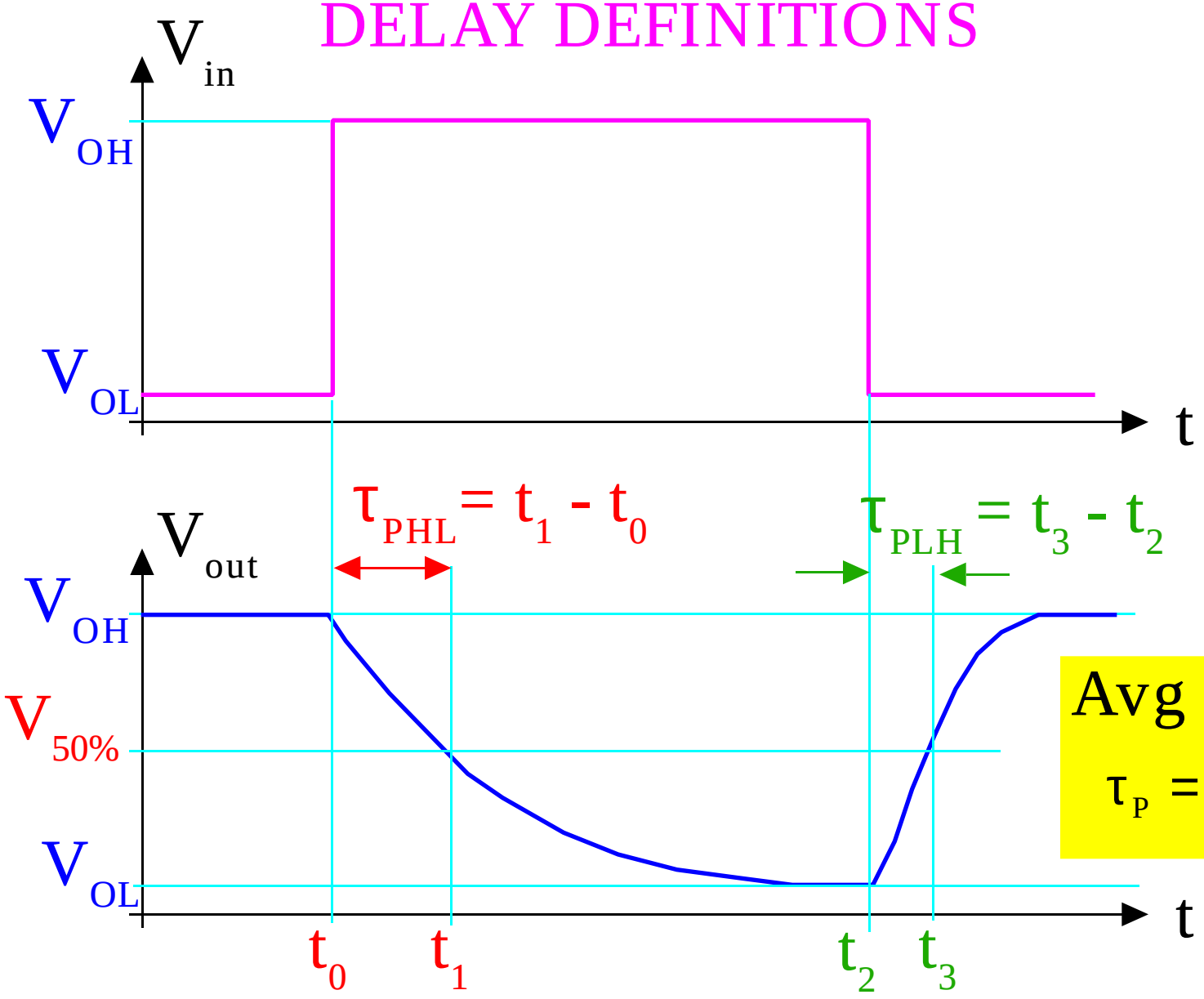
$$C_{load} = C_{gdn}^{\checkmark} + C_{gdp}^{\checkmark} + C_{dbn}^{\checkmark} + C_{dbp}^{\checkmark} + C_{int}^{\checkmark} + C_{gb}^{\checkmark}$$



$$i_C = i_{Dp} - i_{Dn}$$

$$C_{load} = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{int} + C_{gb}$$

DELAY DEFINITIONS

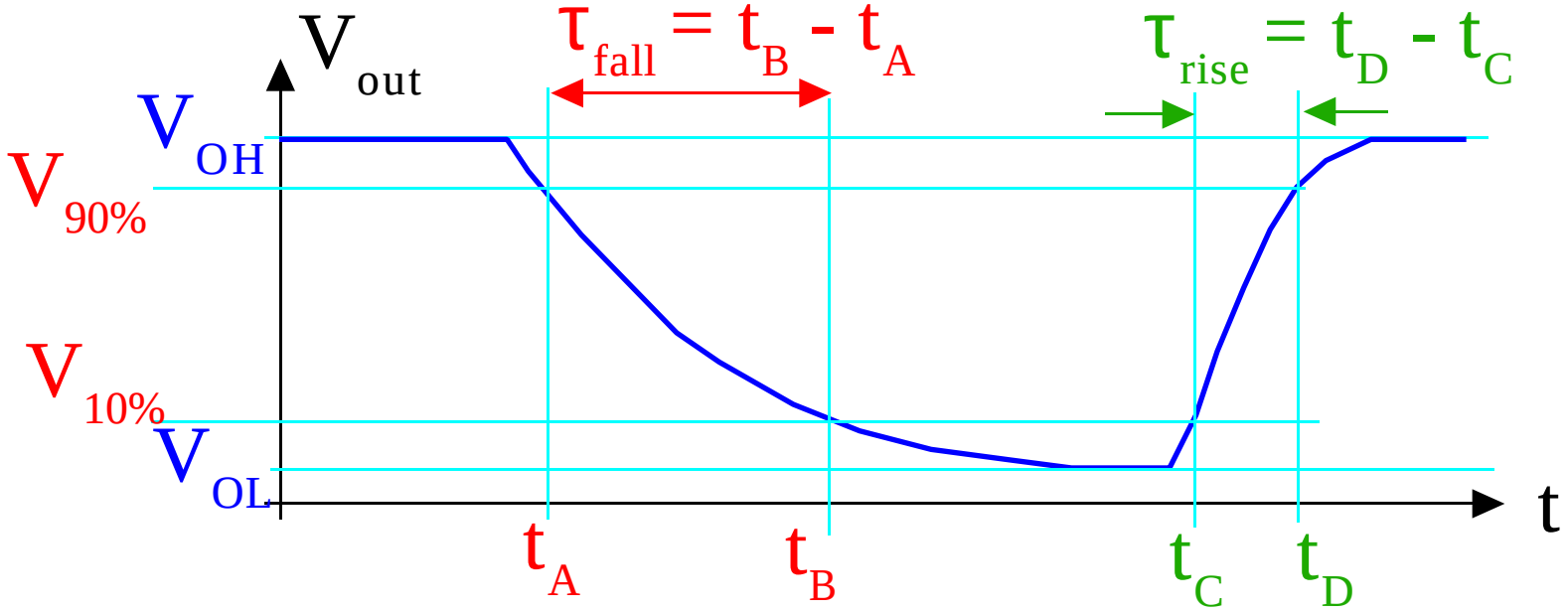


Avg Prop Delay

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

$$V_{50\%} = V_{OL} + 0.5\,[V_{OH} - V_{OL}] = 0.5\,[V_{OL} + V_{OH}]$$

OUTPUT VOLTAGE RISE & FALL TIMES



$$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$$

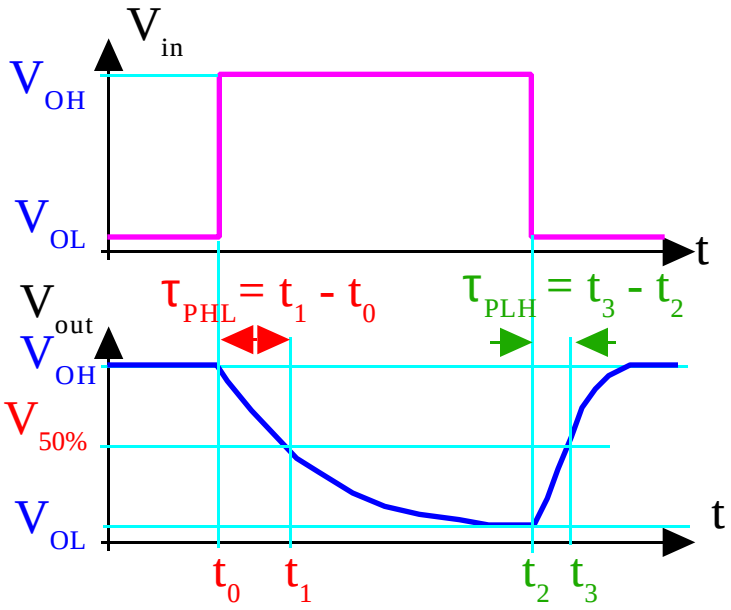
$$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$$

CALCULATION OF DELAY TIMES

QUICK ESTIMATES:

$$\tau_{PHL} = \frac{C_{load}\,\Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load}\left(V_{OH} - V_{50\%}\right)}{I_{avg,HL}}$$

$$\tau_{PLH} = \frac{C_{load}\,\Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load}\left(V_{50\%} - V_{OL}\right)}{I_{avg,LH}}$$



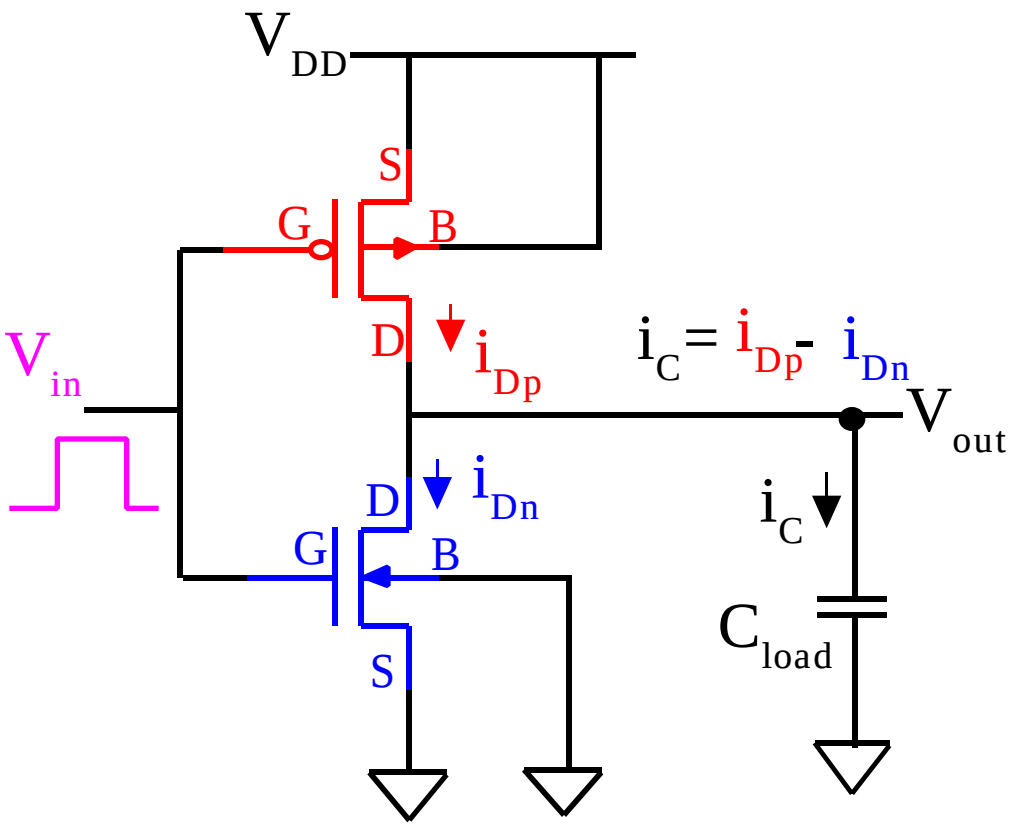
$I_{avg,HL}$ -> approximate average C_{load} current during high-to-low V_{out} transition

$$I_{avg,HL} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{OH}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{50\%}\right)\right]$$

$I_{avg,LH}$ -> approximate average C_{load} current during low-to-high V_{out} transition

$$I_{avg,LH} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OL}, V_{out} = V_{OL}\right) + i_C\left(V_{in} = V_{OL}, V_{out} = V_{50\%}\right)\right]$$

MORE ACCURATE CALCULATION OF τ_{PHL}, τ_{PLH}:



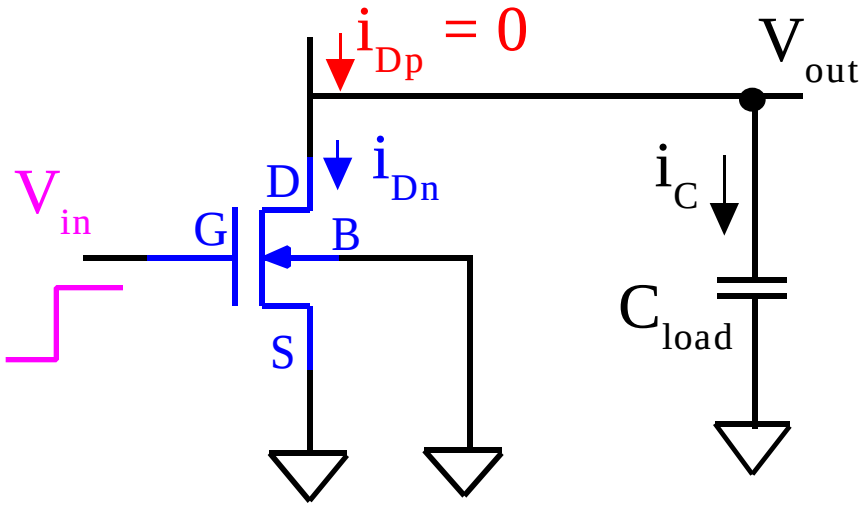
$$i_C = C_{load}\frac{dV_{out}}{dt} = i_{Dp} - i_{Dn}$$

1) V_{in} -RISING CASE:

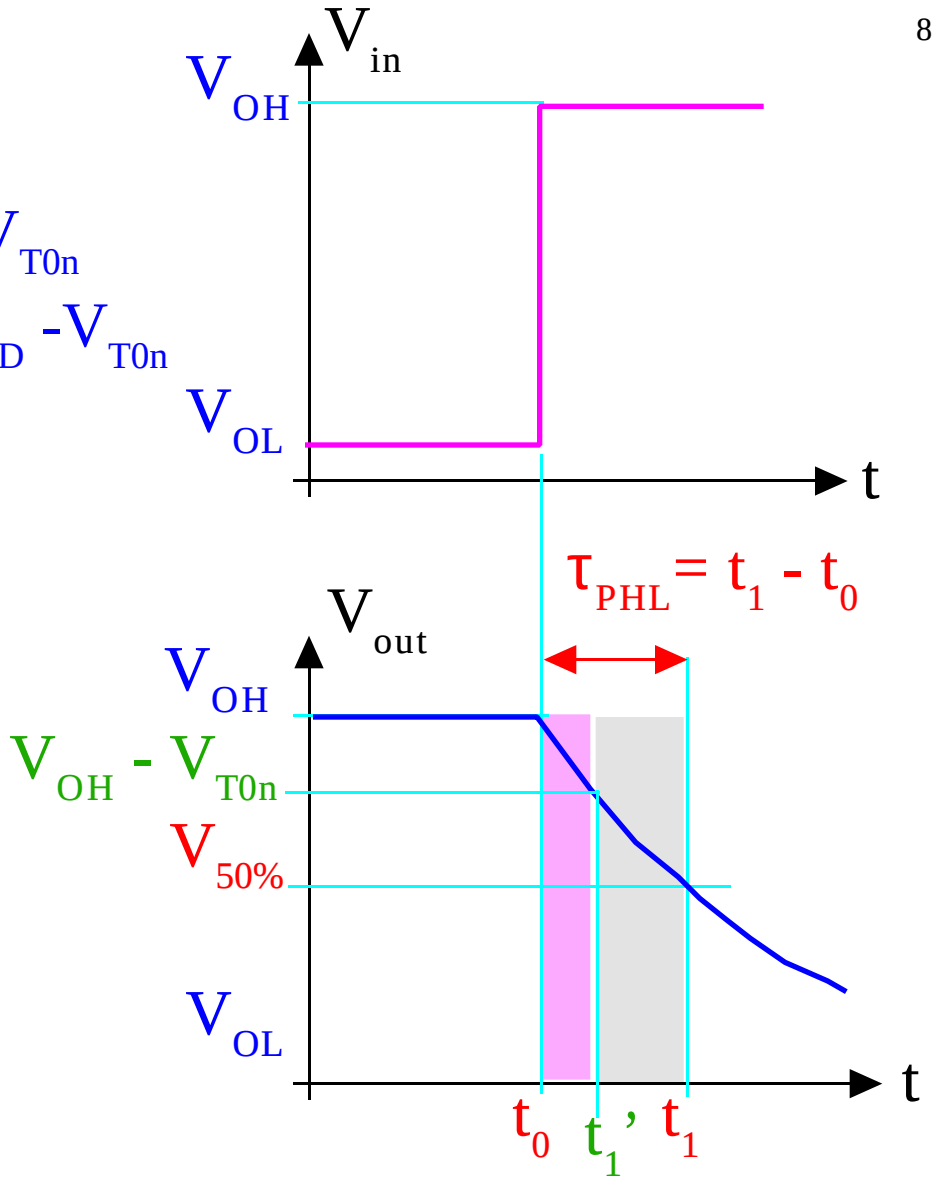
IC: $V_{out} = V_{OH}$, $V_{in} = V_{OL}$ -> V_{OH}

nMOS - ON SAT $V_{out} \geq V_{DD} - V_{T0n}$

p-MOS OFF LIN $0 \leq V_{out} < V_{DD} - V_{T0n}$



$$C_{load}\frac{dV_{out}}{dt} = -i_{Dn}$$

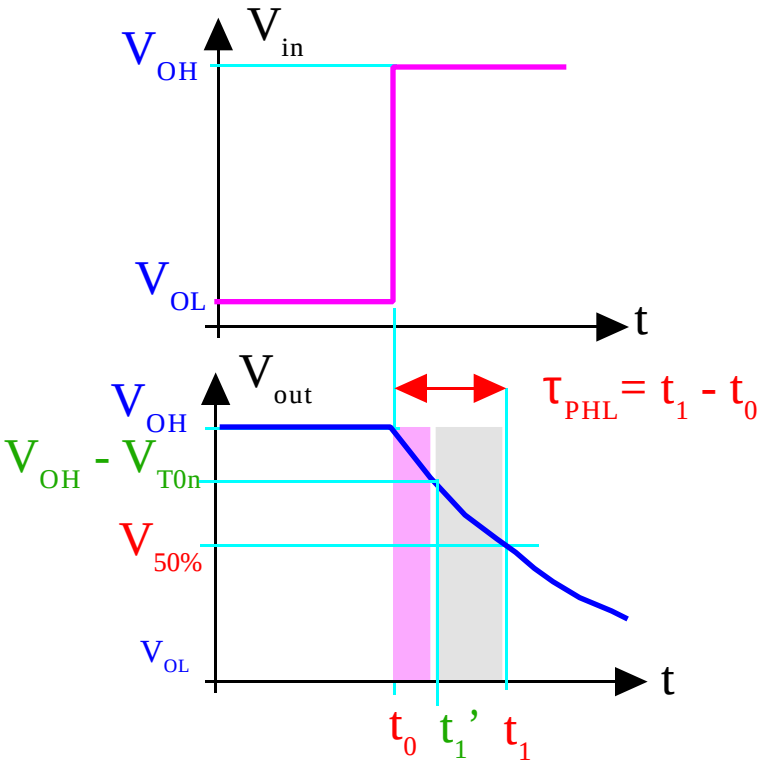


NOTE THAT:

$|i_{Dp}| << |i_{Dn}|$ for all inverter types

nMOS SAT

nMOS LIN



$t_0 < t < t_1'$:

$$i_{Dn} = \frac{k_n}{2}(V_{in} - V_{T0n})^2$$

$$= \frac{k_n}{2}(V_{OH} - V_{T0n})^2 = -C_{load}\frac{dV_{out}}{dt}$$

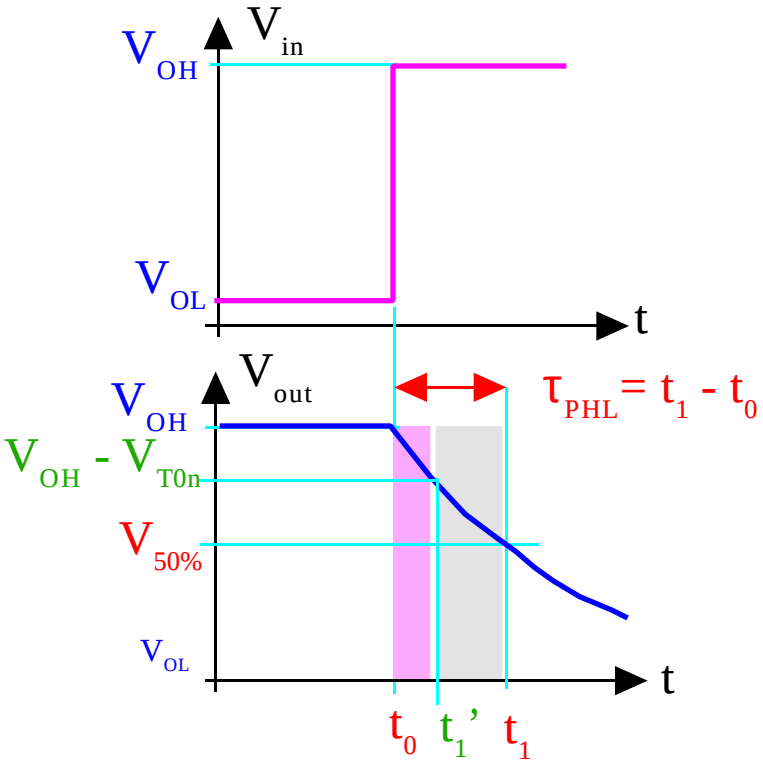
for $V_{OH} - V_{T0n} < V_{out} \geq V_{OH}$

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

Since i_{Dn} is INDEP of V_{out}

$$\int_{t=t_0}^{t=t_1'} dt = -\frac{C_{load}}{\frac{k_n}{2}(V_{OH} - V_{T0n})^2} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} dV_{out}$$

$$t_1' - t_0 = \frac{2C_{load}V_{T0n}}{k_n(V_{OH} - V_{T0n})^2}$$



$t_1' < t < t_1$:

$$i_{Dn} = \frac{k_n}{2}\left[2(V_{in} - V_{T0n})V_{out} - V_{out}^2\right]$$

$$= \frac{k_n}{2}\left[2(V_{OH} - V_{T0n})V_{out} - V_{out}^2\right] = -C_{load}\frac{dV_{out}}{dt}$$

for $V_{out} \le V_{OH} - V_{T0n}$

$$\int_{t=t_1'}^{t=t_1} dt = -C_{load}\int_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

$$\int_{t=t_1'}^{t=t_1} dt = -2C_{load}\int_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}} \left(\frac{1}{k_n\left[2(V_{OH} - V_{T0n})V_{out} - V_{out}^2\right]}\right) dV_{out}$$

$$t_1 - t_1' = -\frac{2C_{load}}{k_n}\frac{1}{2(V_{OH} - V_{T0n})}\ln\left(\frac{V_{out}}{2(V_{OH} - V_{T0n}) - V_{out}}\right)\Bigg|_{V_{out}=V_{OH}-V_{T0n}}^{V_{out}=V_{50\%}}$$

$$t_1 - t_1' = -\frac{2C_{load}}{k_n}\frac{1}{2(V_{OH}-V_{T0n})}\ln\left(\frac{2(V_{OH}-V_{T0n})-V_{out}}{V_{out}}\right)\Bigg|_{\substack{V_{out}=V_{50\%}\\ V_{out}=V_{OH}-V_{T0n}}}$$

$$= \frac{C_{load}}{k_n(V_{OH}-V_{T0n})}\ln\left(\frac{2(V_{OH}-V_{T0n})-V_{50\%}}{V_{50\%}}\right)$$

$$\rightarrow \quad t_1' - t_0 = \frac{2C_{load}V_{T0n}}{k_n(V_{OH}-V_{T0n})^2}$$

$$\tau_{PHL} = t_1 - t_1' + t_1' - t_0$$

$$\tau_{PHL} = \frac{2C_{load}V_{T0n}}{k_n(V_{OH}-V_{T0n})^2} + \frac{C_{load}}{k_n(V_{OH}-V_{T0n})}\ln\left(\frac{2(V_{OH}-V_{T0n})-V_{50\%}}{V_{50\%}}\right)$$

$$= \frac{C_{load}}{k_n(V_{OH}-V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH}-V_{T0n}} + \ln\left(\frac{2(V_{OH}-V_{T0n})}{V_{50\%}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{OH} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{2(V_{OH} - V_{T0n})}{V_{50\%}} - 1\right)\right]$$

SUBSTITUTING $V_{50\%} = 0.5\,[V_{OL} + V_{OH}]$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{OH} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{OH} - V_{T0n}} + \ln\left(\frac{4(V_{OH} - V_{T0n})}{V_{OH} + V_{OL}} - 1\right)\right]$$

WHERE for CMOS Inverters $V_{OL} = 0,\ V_{OH} = V_{DD}$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

EXAMPLE 6.1

Consider a CMOS inverter with C_{load} = 1.0 pF, where the IV characteristics of the nMOS transitor driver are specified as follows:

$$V_{GSn} = 5\ V \text{ and } V_{DSn} \geq 4V \Rightarrow I_{Dn} = I_{Dnsat} = 5\ mA$$

Assume V_{in} is a step pulse that switches instantaneously from 0 to 5 V. Calculate the delay time necessary for the inverter output to fall from its initial value of 5 V to 2.5 V.

$$V_{50\%} = 0.5\,[V_{OL} + V_{OH}] = 0.5\,[0 + 5\ V] = 2.5\ V$$

FROM IV DATA: at SAT $V_{DSn} = 5V - V_{T0n} = 4\ V \Rightarrow V_{T0n} = 1\ V$

$$k_n = \frac{2\,I_{Dnsat}}{(V_{GS} - V_{T0n})^2} = \frac{10\,mA}{(4V)^2} = 0.625 \times 10^{-3}\ A/V^2$$

$t_0 < t < t_1'$:

where $i_{Dn} = I_{Dnsat} = 5mA$

$V_{OH} - V_{T0n} = 4\ V$

$V_{OH} = 5\ V$

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T0n}} \left(\frac{1}{i_{Dn}}\right) dV_{out}$$

$$t_1' - t_0 = -\frac{C_{load}}{I_{Dnsat}} \int_{V_{out}=5V}^{V_{out}=4V} dV_{out} = -\frac{1pF}{5mA}(-1V) = 0.2ns$$

$t_1' < t < t_1$:

$$t_1 - t_1' = \frac{C_{load}}{k_n(V_{OH} - V_{T0n})} \ln\left(\frac{2(V_{OH} - V_{T0n}) - V_{50\%}}{V_{50\%}}\right)$$

$$= \frac{1pF}{(0.625x10^{-3}\ A/V^2)(5-1)V} \ln\left(\frac{2(5-1)V - 2.5V}{2.5V}\right)$$

$$= \frac{1x10^{-12}\ F}{(0.625x10^{-3}\ A/V^2)4V} \ln\left(\frac{5.5}{2.5}\right) = 1.26\ ns$$

$$\tau_{PHL} = 0.2\ ns + 1.26\ ns = 1.46\ ns$$

EXAMPLE 6.2

Consider a CMOS inverter with $C_{load} = 1.0$ pF and $V_{DD} = 5$ V, where the IV characteristics of the nMOS transitor driver are specified as follows:

$$k_n' = \mu_n C_{ox} = 20\ \mu A/V^2,\ (W/L)_n = 10, \text{ and } V_{T0n} = 1.0\ V$$

Use both the average-current method and the differential equation method to calculate τ_{fall} (time elapsed between the time $V_{out} = V_{90\%} = 4.5$ V to the time at which $V_{out} = V_{10\%} = 0.5$ V).

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average-current method

$$I_{avg,fall} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{90\%}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{10\%}\right)\right]$$

(5V, 4.5V, 5V, 0.5V)

$$= \frac{1}{2}\left[\frac{1}{2}k_n\left(V_{in} - V_{T0n}\right)^2 + \frac{1}{2}k_n\left(2(V_{in} - V_{T0n})V_{out} - V_{out}^2\right)\right]$$

$$= \frac{1}{4}k_n\left[\left(V_{OH} - V_{T0n}\right)^2 + \left(2(V_{OH} - V_{T0n})V_{10\%} - V_{10\%}^2\right)\right]$$

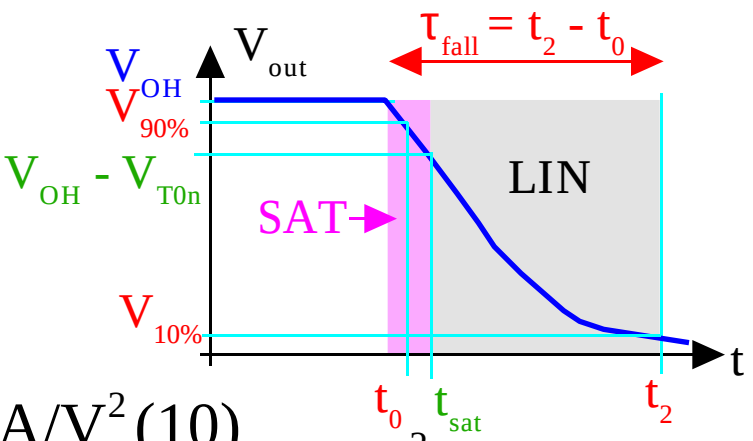
$$= \frac{1}{4}20\text{x}10^{-6}(A/V^2)(10)\left[(5-1)^2\ V^2 + \left(2(5-1)0.5 - (0.5)^2\right)V^2\right] = 0.9875\text{mA}$$

average-current method cont.

$$\tau_{fall} = \frac{C_{load}\,\Delta V}{I_{avg,fall}} = \frac{1\text{x}10^{-12}\,\text{F}(4.5-0.5)\text{V}}{0.9875\text{x}10^{-3}\,\text{A}} = 4.05\text{x}10^{-9}\,\text{s} = 4.09\,\text{ns}$$

differential equation method

SAT for $4.0\,\text{V} \leqslant V_{out} \leqslant 4.5\,\text{V}$



$$C_{load}\frac{dV_{out}}{dt} = -\frac{1}{2}k_n\left(V_{in}-V_{T0n}\right)^2$$

$V_{OH} = 5\,\text{V}$

$$\frac{dV_{out}}{dt} = -\frac{k_n}{2\,C_{load}}\left(V_{in}-V_{T0n}\right)^2 = -\frac{20\text{x}10^{-6}\,\text{A/V}^2(10)}{2(1\text{x}10^{-12}\,\text{F})}(5-1)^2$$

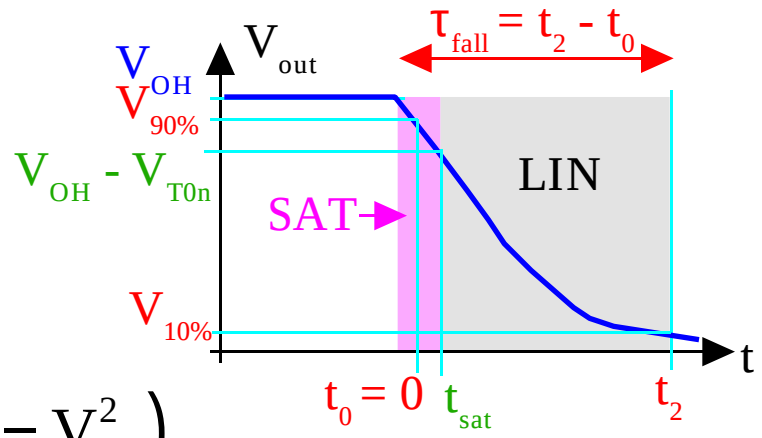
$$= -1.6\text{x}10^{-9}\,\text{V/s}$$

$$\int_{t=t_0}^{t=t_{sat}} dt = -\frac{1}{1.6\text{x}10^{-9}\,\text{V/s}}\int_{V_{out}=4.5\text{V}}^{V_{out}=4.0\text{V}} dV_{out}$$

$$t_{sat} - t_0 = -\frac{1}{1.6\text{x}10^{-9}\,\text{V/s}}V_{out}\Big|_{V_{out}=4.5\text{V}}^{V_{out}=4.0\text{V}} = -\frac{1}{1.6\text{x}10^{-9}\,\text{V/s}}(4.0-4.5)\text{V}$$

$$t_{sat} - t_0 = 0.3125\ \text{ns}$$

differential equation method cont



$t_{sat} = 0.3125$ ns

LIN for $0.5\text{ V} \leq V_{out} < 4.0\text{ V}$

$$C_{load}\frac{dV_{out}}{dt} = -\frac{1}{2}k_n\left(2(V_{in}-V_{T0n})V_{out}-V_{out}^2\right)$$

$$\int_{t=t_{sat}}^{t=t_2} dt = -2C_{load}\int_{V_{out}=4.0\text{ V}}^{V_{out}=0.5\text{ V}} \frac{dV_{out}}{k_n\left(2(V_{in}-V_{T0n})V_{out}-V_{out}^2\right)}$$

$$t_2 - t_{sat} = \frac{C_{load}}{k_n}\frac{1}{(V_{in}-V_{T0n})}\ln\left(\frac{2(V_{in}-V_{T0n})-V_{10\%}}{V_{10\%}}\right)$$

$V_{OH} = 5$ V (numerator)

$V_{OH} = 5$ V (denominator)

$$= \frac{1\text{x}10^{-12}\text{ F}}{20\text{x}10^{-6}\text{ A/V}^2(10)}\frac{1}{(5-1)\text{V}}\ln\left(\frac{2(5-1)-0.5}{0.5}\right) = 3.385\text{ ns}$$

$$\tau_{fall} = (t_2 - t_{sat}) + (t_{sat} - t_0) = 3.385\text{ns} + 0.3125\text{ns} = 3.6975\text{ns}$$

= 4.09 ns I_{avg} method

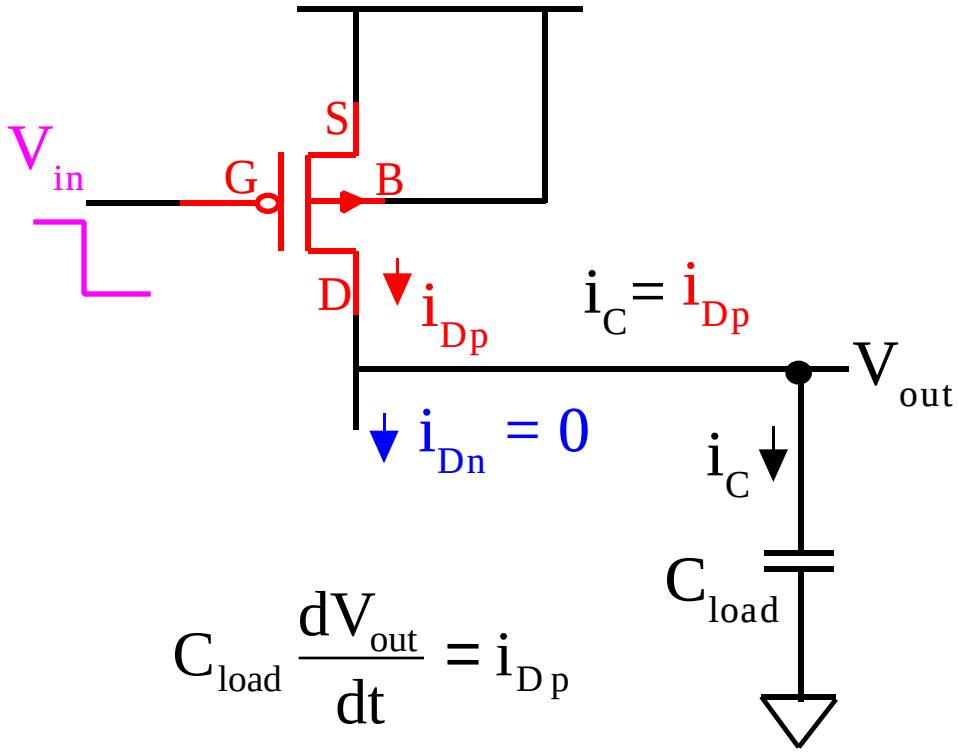
2) V_{in} -FALLING CASE:

IC: $V_{out} = V_{OL}$, $V_{in} = V_{OH}$ -> V_{OL}

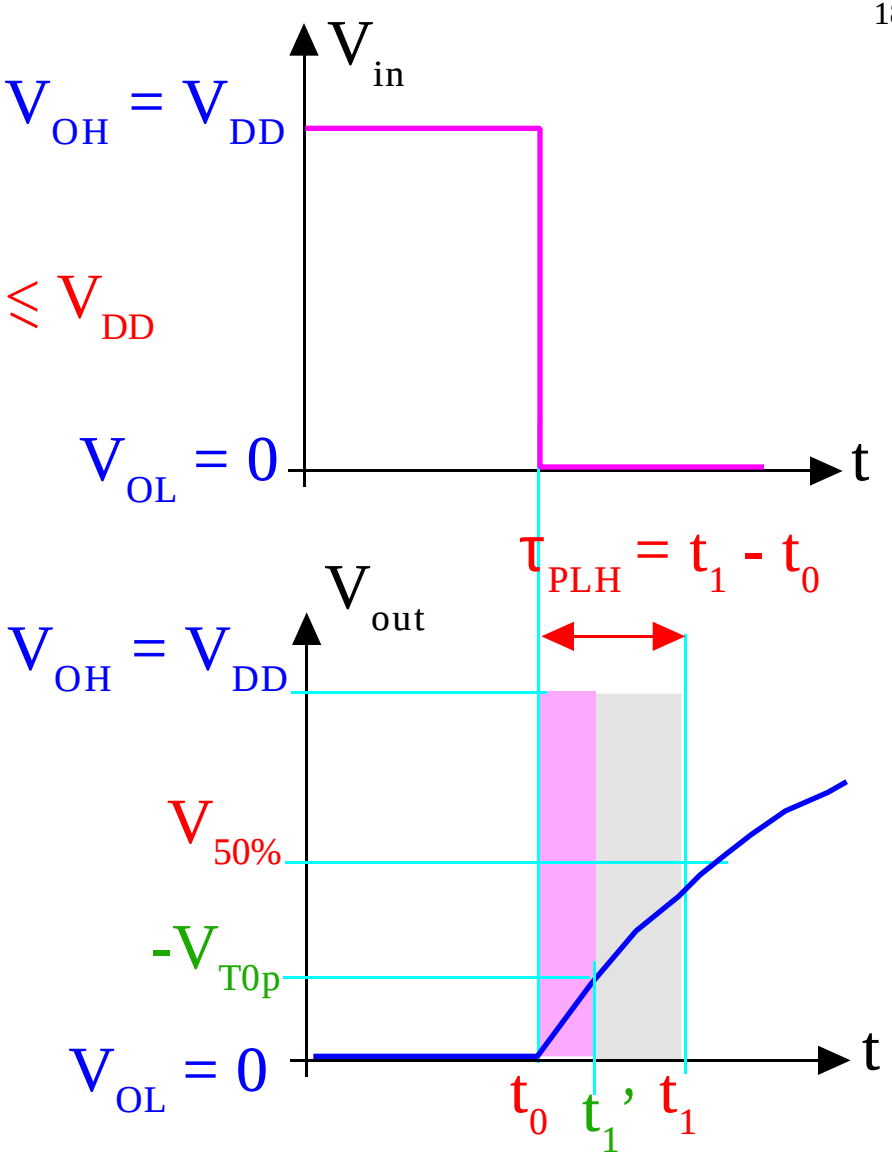
nMOS - OFF SAT $V_{out} \leq -V_{T0p}$

p-MOS ON LIN $-V_{T0p} < V_{out} \leq V_{DD}$

$V_{GS} = V_{in} - V_{DD}$ $V_{DS} = V_{out} - V_{DD}$



$$C_{load}\frac{dV_{out}}{dt} = i_{Dp}$$



$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{OH} - V_{OL} - |V_{T0p}|)} \left[\frac{2|V_{T0p}|}{V_{OH} - |V_{T0p}|} + \ln\left(\frac{2(V_{OH} - V_{OL} - |V_{T0p}|)}{V_{OH} - V_{50\%}} - 1 \right) \right]$$

$V_{50\%} = 0.5\,[V_{OL} + V_{OH}]$, FOR CMOS INV: $V_{OL} = 0$, $V_{OH} = V_{DD}$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)} \left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{2(V_{OH} - V_{T0n})}{V_{50\%}} - 1 \right) \right]$$

FOR CMOS INV: $V_{OL} = 0$, $V_{OH} = V_{DD}$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})} \left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1 \right) \right]$$

CONDITIONS FOR Balanced CMOS Inverter Propagation Delays, i.e. $\tau_{PHL} = \tau_{PLH}$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

where $k_n = \mu_n C_{ox}\frac{W_n}{L_n}$ & $k_p = \mu_p C_{ox}\frac{W_p}{L_p}$

FOR $\tau_{PHL} = \tau_{PLH}$

$V_{T0n} = |V_{T0p}|$

$k_n = k_p$ or $\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n}$

NOTE THAT:

- Calculation of τ_{PHL}, depends largely on NMOS driver, i.e. nearly same for all INV types.
- Calculation of τ_{PLH}, depends largely on the load device and its operation, i.e. different for all INV types.

CONSIDER depletion NMOS Load:

$$C_{load}\frac{dV_{out}}{dt} = i_{D,L}(V_{out})$$

$$V_{T,L} = V_{T0,L} + \gamma\left(\sqrt{|2\varphi_F| + V_{out}} - \sqrt{|2\varphi_F|}\right)$$

SAT: $V_{DS,L} = V_{DD} - V_{out} \geq 0 - V_{T,L}$ => $V_{out} \leq V_{DD} + V_{T,L}$

$$I_{D,L} = \frac{k_{n,L}}{2}\left[-V_{T,L}(V_{out})\right]^2$$

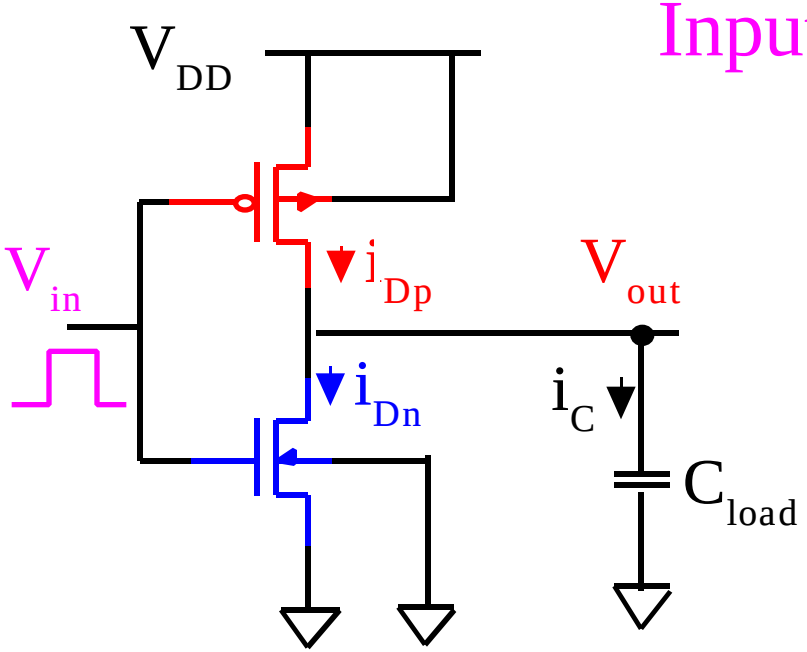
LIN: $V_{DS,L} = V_{DD} - V_{out} < 0 - V_{T,L}$ => $V_{out} > V_{DD} + V_{T,L}$

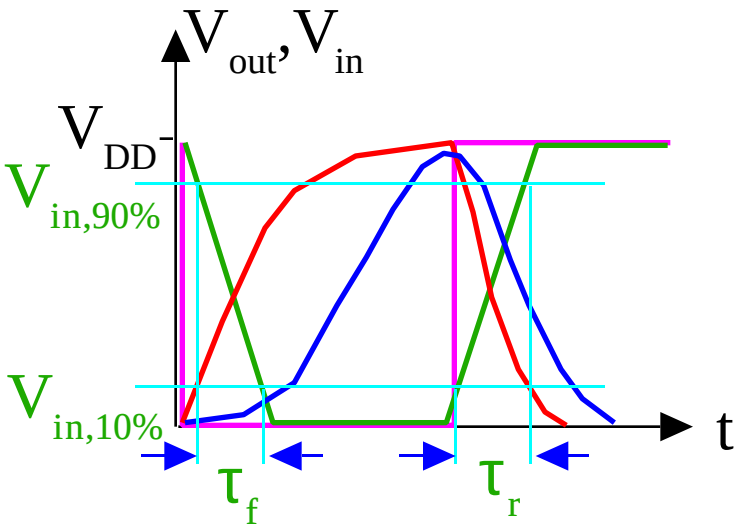
$$I_{D,L} = \frac{k_{n,L}}{2}\left[2(-V_{T,L}(V_{out}))(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right]$$

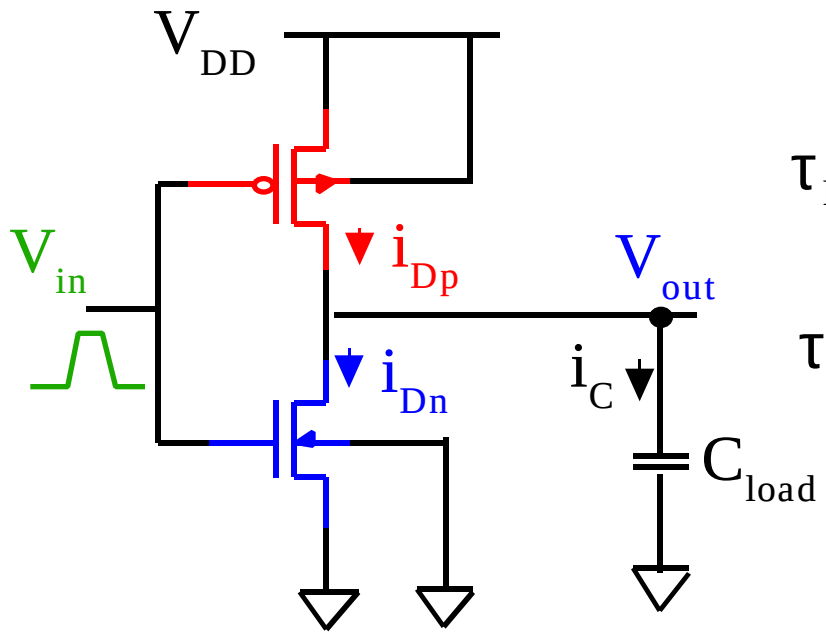
$$\tau_{PLH} = C_{load}\left[\int_{V_{out}=V_{OL}}^{V_{out}=V_{DD}-|V_{T,L}|}\left(\frac{dV_{out}}{i_{D,L}(sat)}\right) + \int_{V_{out}=V_{DD}-|V_{T,L}|}^{V_{out}=V_{50\%}}\left(\frac{dV_{out}}{i_{D,L}(lin)}\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_{n,L}|V_{T,L}|}\left[\frac{2\left(V_{DD}-|V_{T,L}|-V_{OL}\right)}{|V_{T,L}|} + \ln\left(\frac{2|V_{T,L}|-(V_{DD}-V_{50\%})}{V_{DD}-V_{50\%}}\right)\right]$$

Input Waveform Slope







EMPERICAL DELAY CORRECTIONS FOR INPUT τ_r, τ_f:

$$\tau_{PHL}(\text{actual}) = \sqrt{\tau_{PHL}^2(\text{step}-\text{input}) + \left(\frac{\tau_r}{2}\right)^2}$$

$$\tau_{PLH}(\text{actual}) = \sqrt{\tau_{PLH}^2(\text{step}-\text{input}) + \left(\frac{\tau_f}{2}\right)^2}$$

INVERTER DELAY DESIGN FORMULAS

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

where $k_n = \mu_n C_{ox}\frac{W_n}{L_n}$

$$\frac{W_n}{L_n} = \frac{C_{load}}{\tau_{PHL}\mu_n C_{ox}(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

where $k_p = \mu_p C_{ox}\frac{W_p}{L_p}$

$$\frac{W_p}{L_p} = \frac{C_{load}}{\tau_{PLH}\mu_p C_{ox}(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{4(V_{DD} - |V_{T0p}|)}{V_{DD}} - 1\right)\right]$$

EXAMPLE 6.3

Design a CMOS inverter by determining the W_n and W_p of the nMOS and PMOS transistors to meet the following specs:

-> $V_{th} = 2$ V for $V_{DD} = 5$ V

-> Delay time of 2 ns for a V_{out} transition from 4 V to 1 V, with $C_{load} = 1.0$ pF.

The process and device parameters are specified as follows:

$k_n' = \mu_n C_{ox} = 30\ \mu A / V^2$,

$k_p' = \mu_p C_{ox} = 10\ \mu A / V^2$

$L_n = L_p = 1.0\ \mu m$

$V_{T0n} = 1.0$ V

$V_{T0p} = -1.5$ V

$W_{min} = 2\ \mu m$ (limited by design rules)

STEP #1: Satisfy the Delay Constraint: τ_{PHL} from 4 V to 1 V

HL => PULL-DOWN => τ_{PHL} determined by nMOS driver

NOTE $V_{in} = V_{OH}$ and $1 \leq V_{out} \leq 4$ V => nMOS LIN

$$C_{load}\frac{dV_{out}}{dt} = -\frac{\mu_n C_{ox}}{2}\frac{W_n}{L_n}\left[2(V_{OH} - V_{T0\,n})V_{out} - V_{out}^2\right]$$

$$\tau_{delay} = 2.0\,x10^{-9}\,s = -2\,C_{load}\frac{1}{\mu_n C_{ox}\frac{W_n}{L_n}}\int_{V_{out}=4}^{V_{out}=1}\frac{dV_{out}}{\left[2(V_{OH} - V_{T0\,n})V_{out} - V_{out}^2\right]}$$

$$= -2\,C_{load}\frac{1}{\mu_n C_{ox}\frac{W_n}{L_n}}\frac{1}{2(V_{OH} - V_{T0\,n})}\ln\left[\frac{V_{out}}{2(V_{OH} - V_{T0\,n}) - V_{out}}\right]_{V_{out}=4}^{V_{out}=1}$$

$$= \frac{-C_{load}}{\mu_n C_{ox}\frac{W_n}{L_n}(V_{DD} - V_{T0n})}\left\{\ln\left[\frac{1V}{2(5-1)V - 1V}\right] - \ln\left[\frac{4V}{2(5-1)V - 4V}\right]\right\}$$

$$2.0x10^{-9}\,s = \frac{-1x10^{-12}\,F}{\left(30x10^{-6}\,A/V^2\right)\frac{W_n}{L_n}(5-1)V}\left\{\ln\left[\frac{1}{7}\right] - \ln\left[\frac{4}{4}\right]\right\}$$

$$\frac{W_n}{L_n} = \frac{1x10^{-12}\,F}{(2.0\,x10^{-9}\,s)(30\,x10^{-6}\,A/V^2)(4)}\ln(7) = \frac{1}{(2.0)(0.03)(4)}\ln(7) = 8.108$$

$$\frac{W_n}{L_n} = 8.108,\ L_n = 1\mu m \quad \Rightarrow \quad W_n = 8.108\,(1\ \mu m) = 8.1\ \mu m$$

From τ_{delay} spec.

STEP #2: Satisfy the V_{th} constraint, where:

$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{1}{k_R}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} = \frac{1.0\,V + \sqrt{\frac{1}{k_R}}(5 + (-1.5))\,V}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

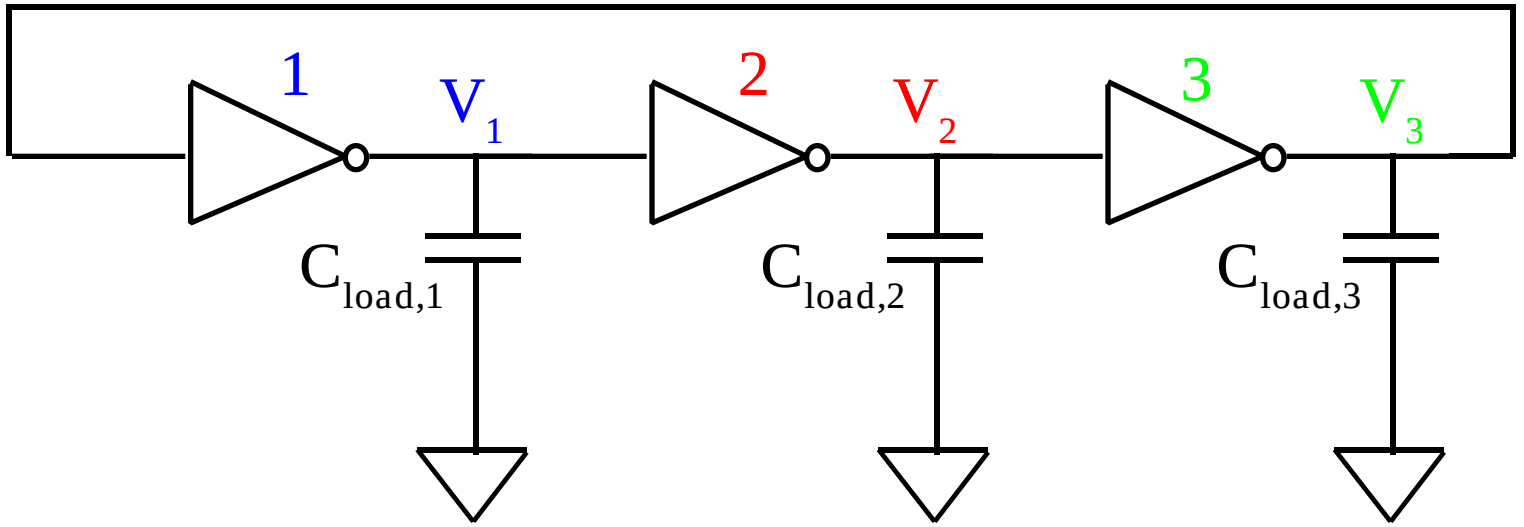
$$= \frac{1.0\,V + \sqrt{\frac{1}{k_R}}(3.5)\,V}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} = 2\,V \quad \Rightarrow \quad k_R = (1.5)^2 = \frac{9}{4}$$

$$k_R = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{30\,W_n}{10\,W_p} = 3\frac{W_n}{W_p} = \frac{9}{4} \quad \Rightarrow \quad W_p = \frac{4}{9}(3)W_n$$

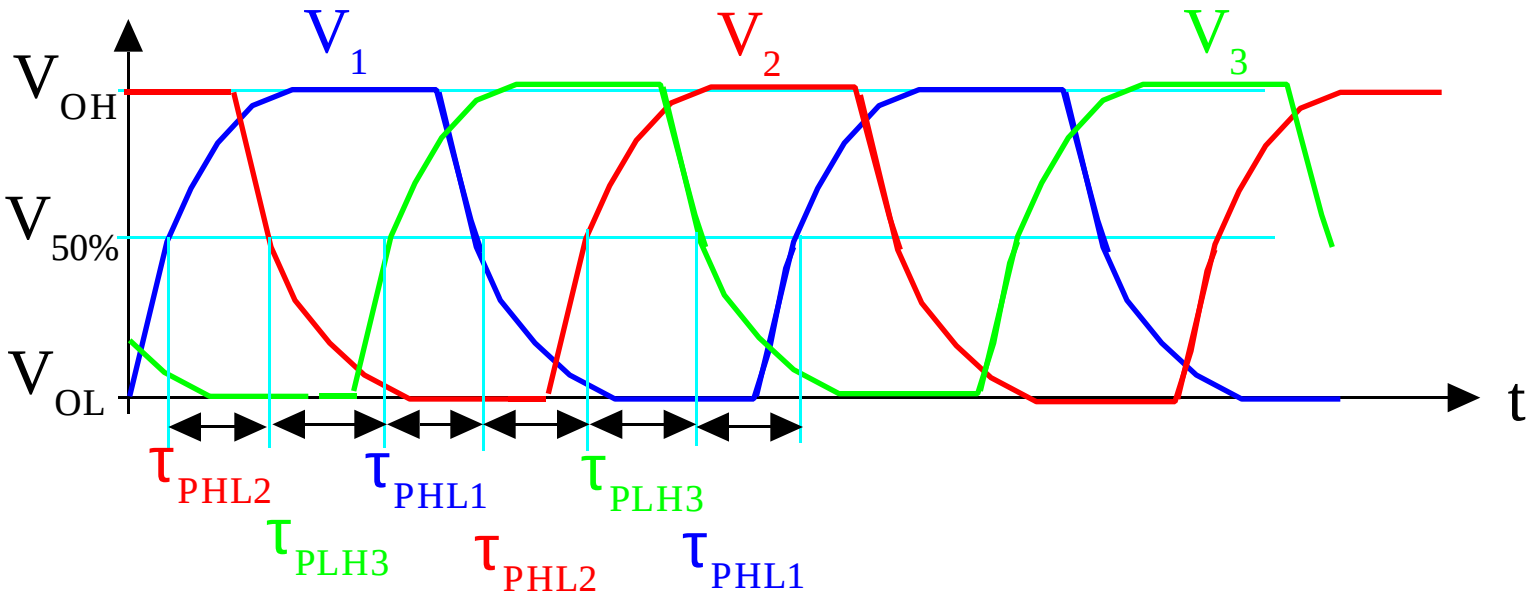
with $L_p = 1\ \mu m$

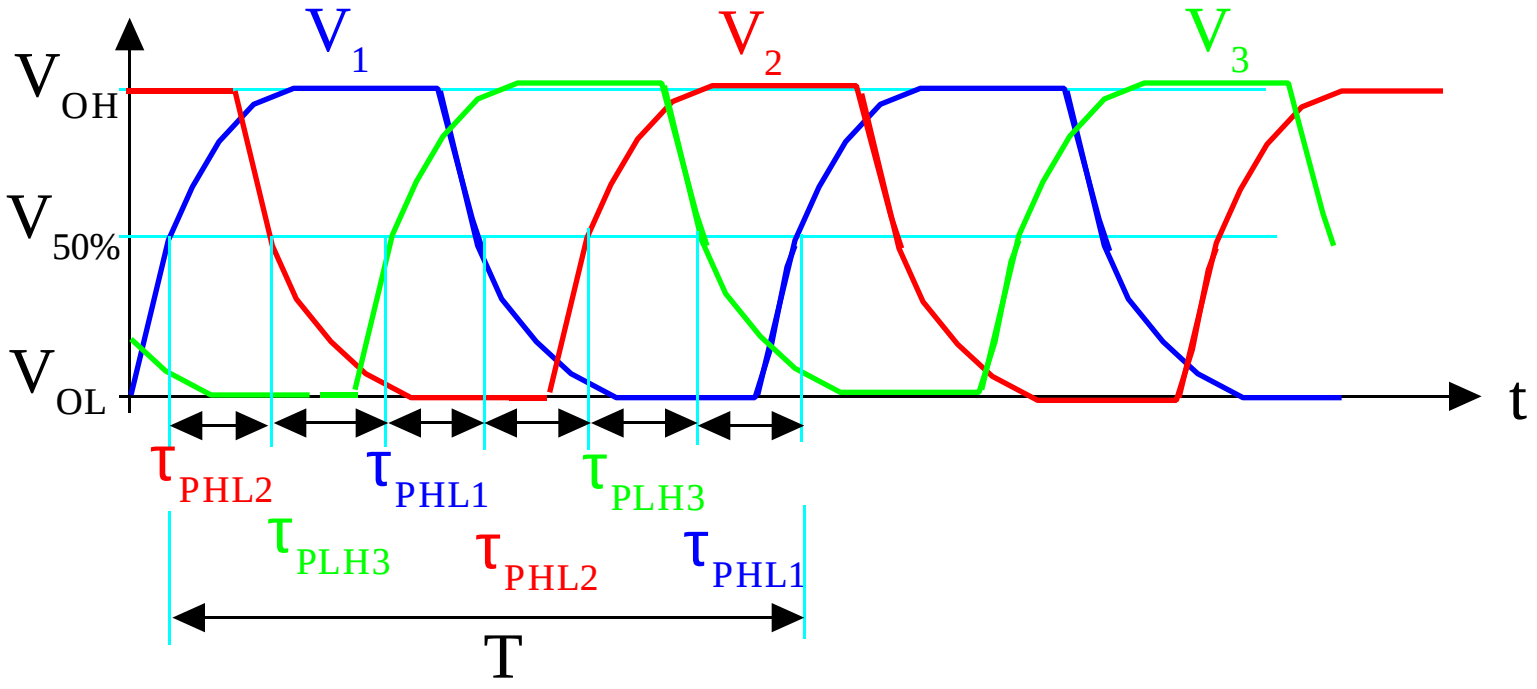
$$W_p = \frac{4}{9}(3)8.1\mu m = 10.8\mu m$$

CMOS RING OSCILLATOR



$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3





$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3

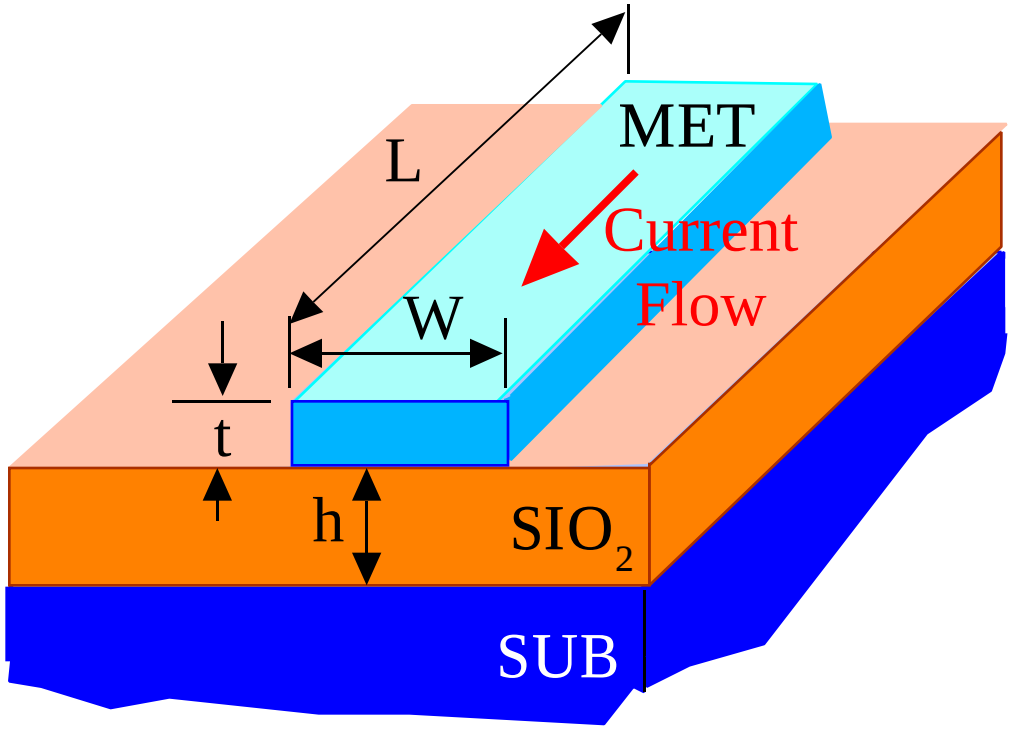
$$T = \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} + \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} = 6\tau_P$$

$$f = \frac{1}{T} = \frac{1}{2(3)\tau_P} = \frac{1}{6\tau_P}$$ Oscillation FREQ

For n INVERTERS:

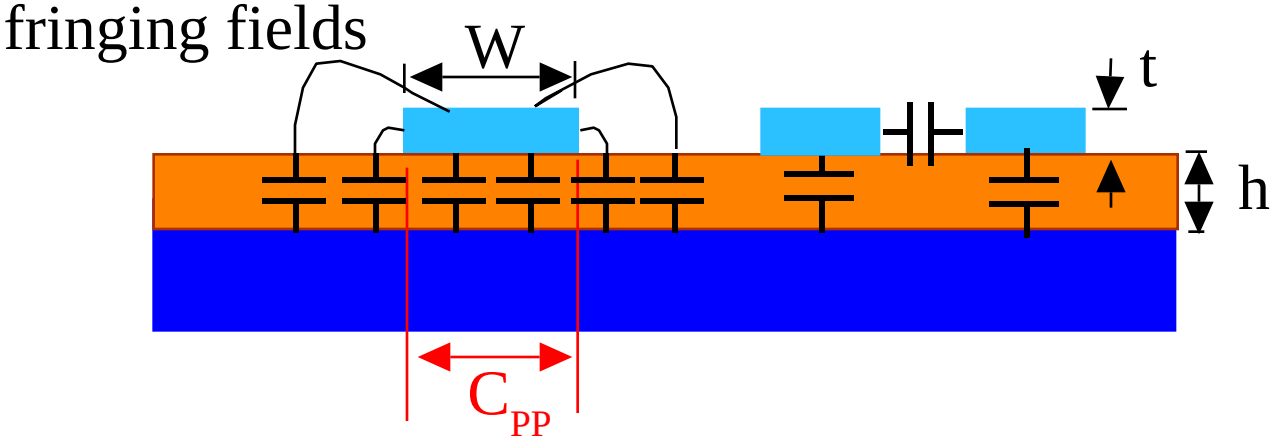
$$f = \frac{1}{T} = \frac{1}{2n\tau_P} \quad \text{or} \quad \tau_P = \frac{1}{2nf}$$

ESTIMATION OF INTERCONECT PARASITICS



PARASITIC RESISTANCE:

$$R_{metal} = \rho \frac{L}{Wt} = R_{sheet} \frac{L}{W}$$



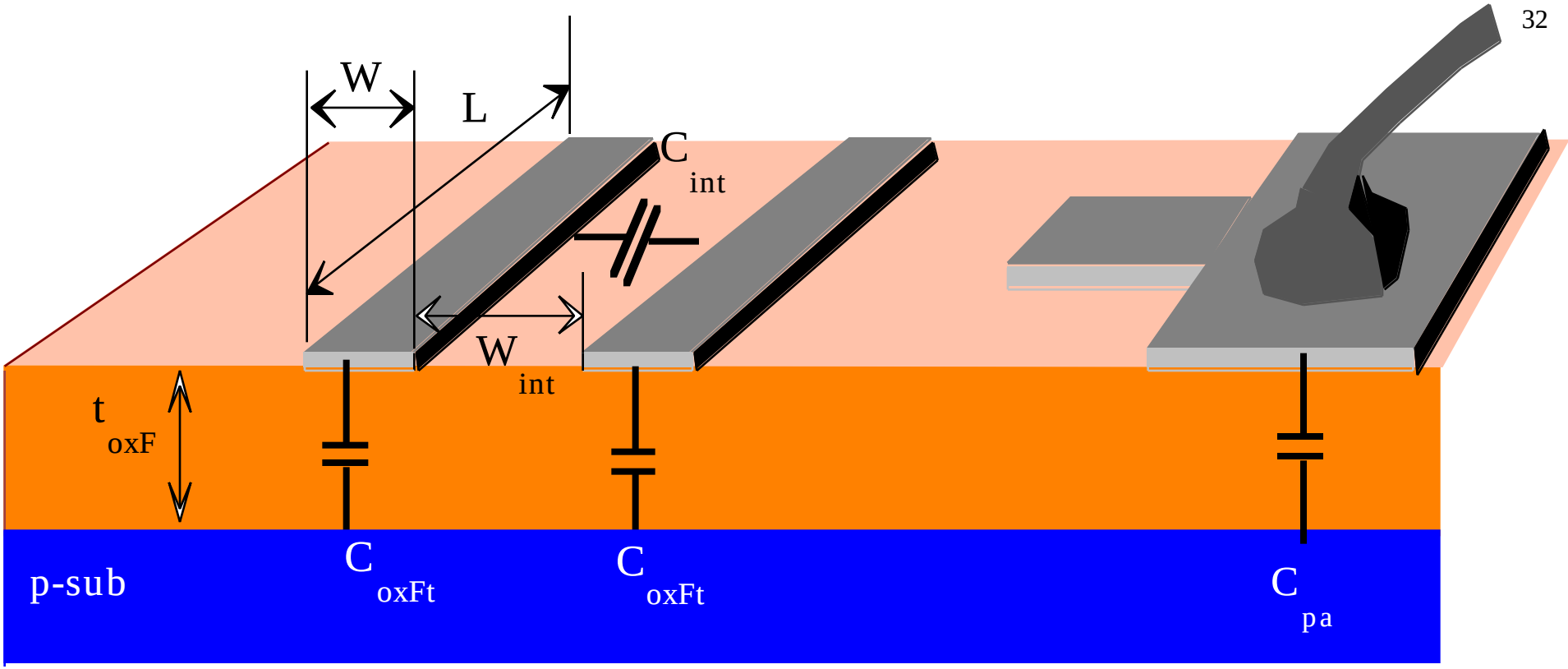
$FF = C_{total}/C_{PP}$ -> FRINGING-FIELD FACTOR

FF -> INC as t/h -> INC, W/h <- DEC, and W/L -> INC

(SEE PLOT FF in FIG. 6.18 of TEXT)

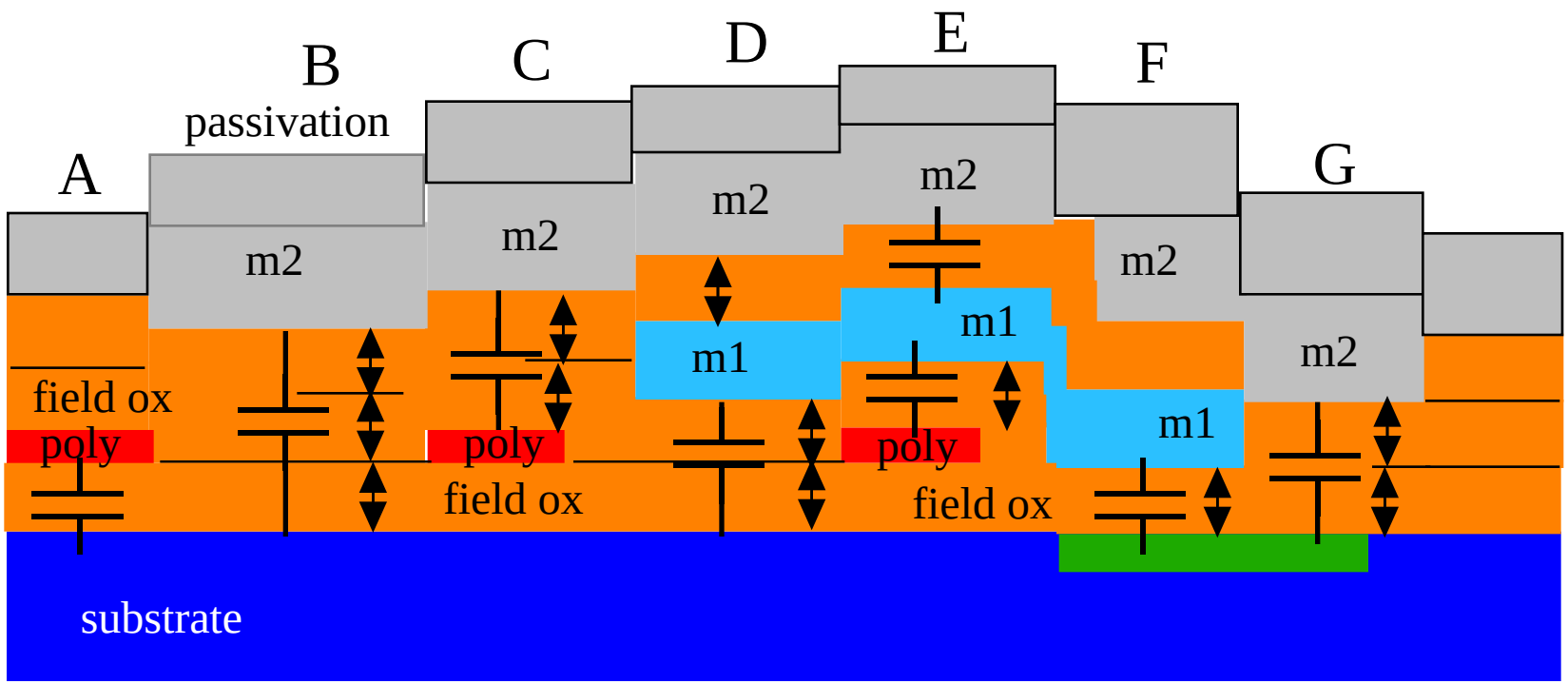
$$C_{total} = \varepsilon\left[\frac{W-\frac{t}{2}}{h} + \frac{2\pi}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left(\frac{2h}{t}+2\right)}\right)}\right] \text{ pF/μm L} \quad \text{for } W \geq t/2$$

$$C_{total} = \varepsilon\left[\frac{W}{h} + \frac{\pi\left(1-0.0543\frac{t}{2h}\right)}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left(\frac{2h}{t}+2\right)}\right)} + 1.47\right] \text{ pF/μm L} \quad \text{for } W < t/2$$



Double-metal double-poly n-well CMOS process

C_{mm}	$C_{metal\text{-}to\text{-}metal}$	=	$2.5\ nF/cm^2$
C_{oxm}	$C_{metal\text{-}to\text{-}substrate}$	=	$5.2\ nF/cm^2$
C_{oxp}	$C_{poly\text{-}to\text{-}substrate}$	=	$6.5\ nF/cm^2$
C_{mm}	$C_{metal\text{-}to\text{-}poly}$	=	$12.0\ nF/cm^2$



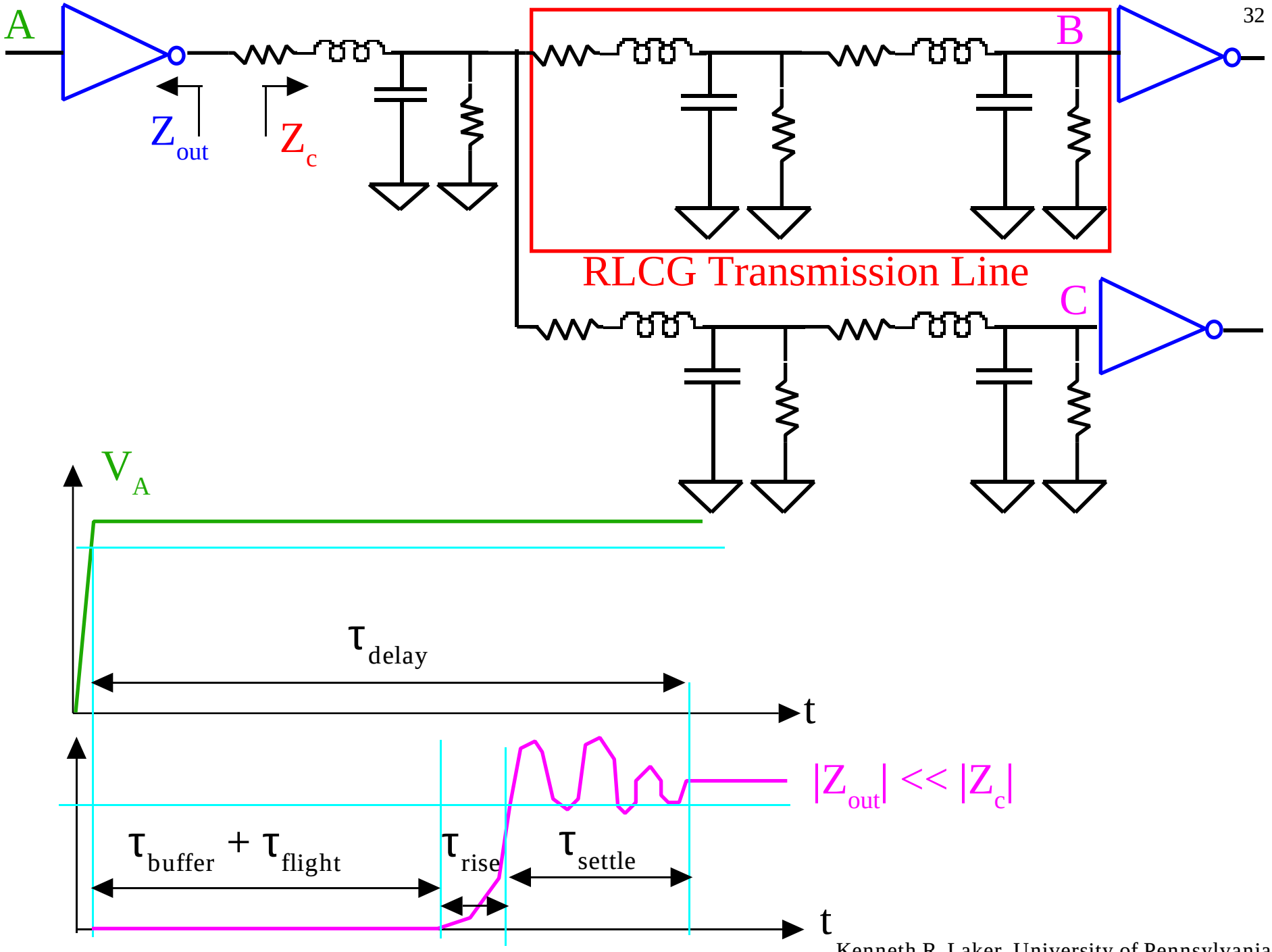
	Layer	Cap	Ox Thickness	Typ Value
A	Poly-substrate	C_p	3000 Å	50 aF/μm²
B	Metal2-sub	C_{m2}	9000 Å	20 aF/μm²
C	Poly-metal2	C_{m2p}	6000 Å	30 aF/μm²
D	Metal1-sub	C_{m1}	6000 Å	30 aF/μm²
E	Metal1-poly	C_{m1p}	3000 Å	60 aF/μm²
E	Metal1-metal2	C_{m2m1}	6000 Å	50 aF/μm²
F	Metal1-diffusion	C_{m1d}	3000 Å	60 aF/μm²
G	Metal2-diffusion	Passivation	6000 Å	30 aF/μm²

1 μm CMOS Capacitances

t_{ox} = 200Å

C_g = 1800 aF/μm²

aF = 10^{-18} F


A
B
C
Z_{out}
Z_c
RLCG Transmission Line
V_A
τ_{delay}
t
$|Z_{out}| << |Z_c|$
$\tau_{buffer} + \tau_{flight}$
τ_{rise}
τ_{settle}
t

ROUTE-LENGTH DESIGN GUIDE

Node: a region of connected paths where the delay associated with signal prop is small compared to gate delays.

To ignore the RC delay of interconnect, $\tau_W << \tau_{Pgate}$ $\quad \tau_W \approx 0.7\frac{rcL_W^2}{2}$

$$\tau_W \approx 0.7\frac{rcL_W^2}{2} << \tau_{Pgate} \Rightarrow L_W << \sqrt{\frac{2\tau_{Pgate}}{0.7(rc)}}$$

L = length of route
r = sheet resistance
c = cap per unit length

EXAMPLE: Consider a minimum width metal1 route to a node with an associated gate delay of 200 ps.

$$L_W << \sqrt{\frac{2\tau_{Pgate}}{0.7(rc)}} = \sqrt{\frac{2x(0.2x10^{-9}s)}{0.7\left(\frac{0.05\Omega}{\lambda}\right)\left(\frac{30x10^{-18}F}{\lambda}\right)}}$$

$$<< 19,518\lambda$$

Conservatively, $L_W < 5000\lambda$

λ = design rule parameter

GUIDELINES FOR IGNORING RC DELAYS (Weste, pp 205)

Layer	Max Length (L_W)
metal3	10,000
metal2	8000
metal1	5000
silicide	600
poly	200
diffusion	60

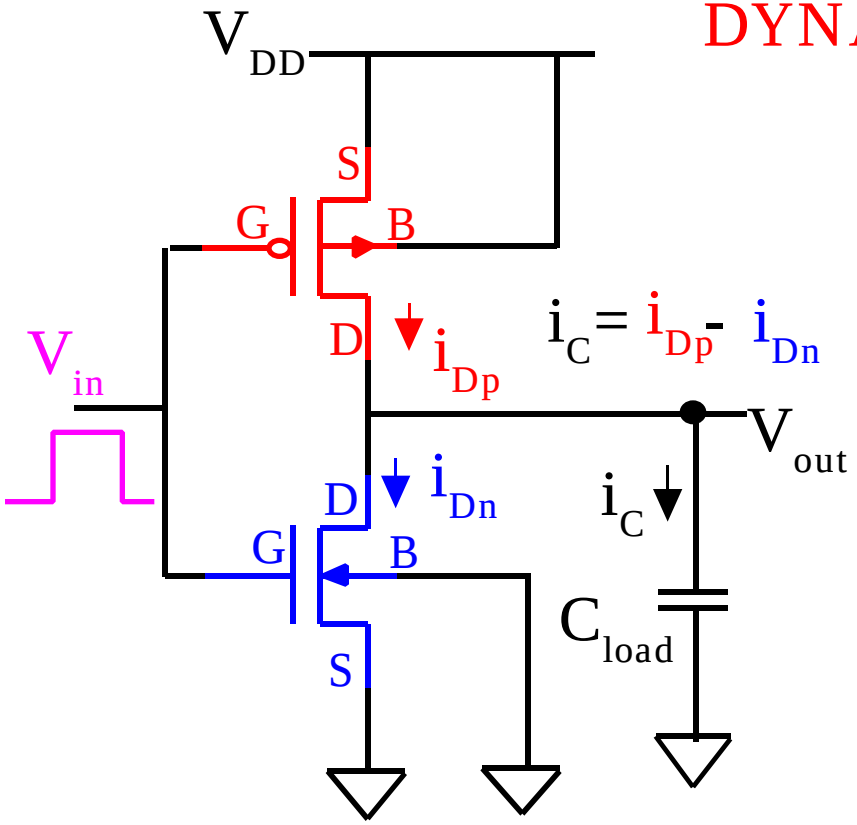
POWER DISSIPATION

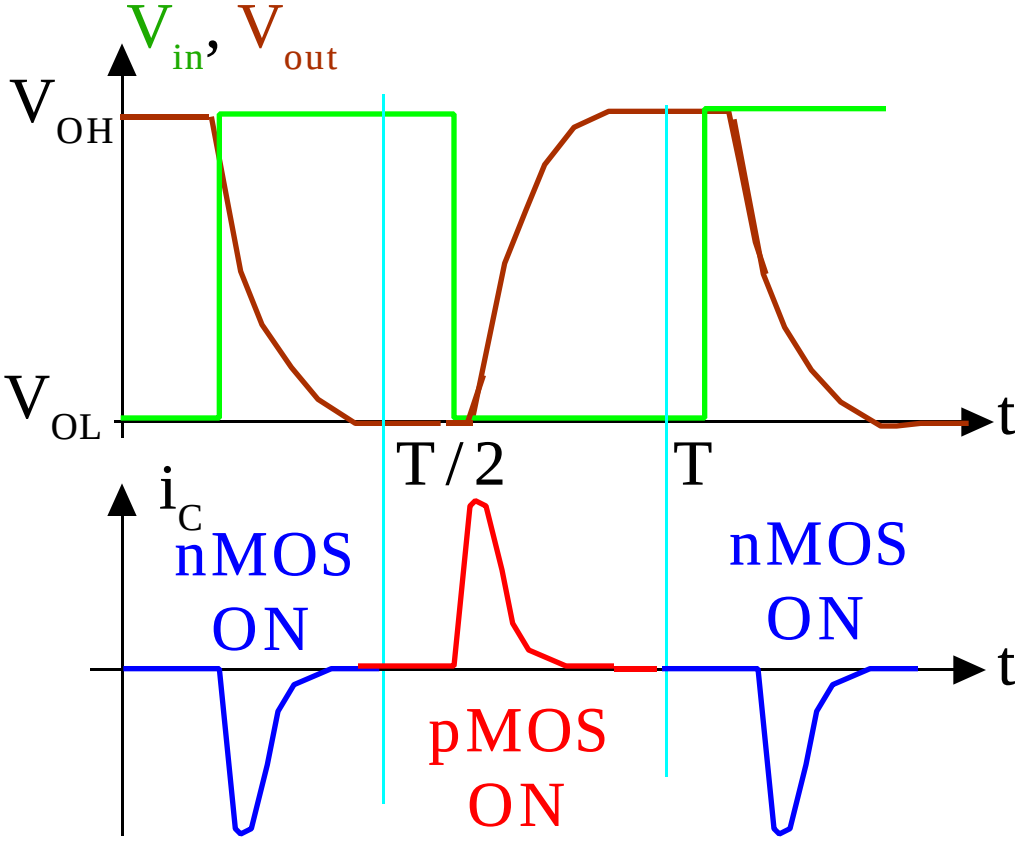
P_s = Static power dissipation due to leakage current or other current drawn continuously from the power supply.

P_d = dynamic power dissipation due to charging and discharging load capacitances (v_{in} assumed to be square-like)

P_{sc} = short circuit power dissipation due to charging and discharging load capacitances during the inite rise and fall times of v_{in}.

DYNAMIC POWER DISSAPATION



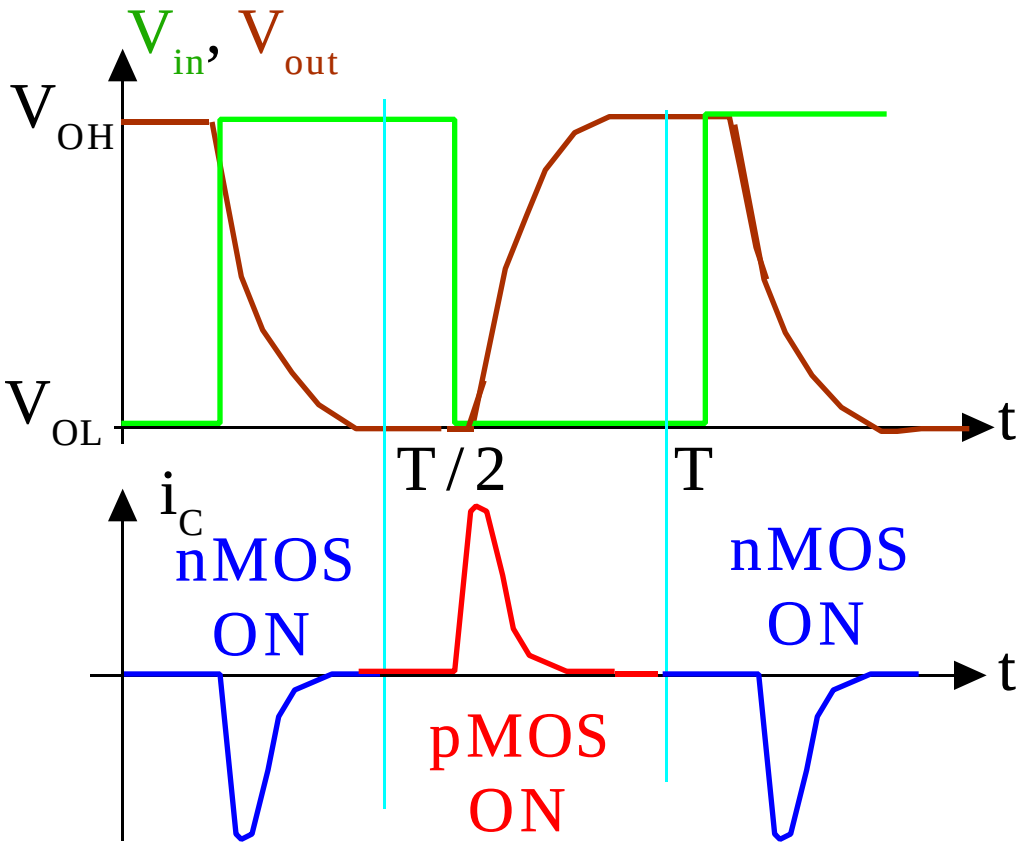


$$P_d = \frac{1}{T}\int_0^T v(t)i(t)dt$$

$$P_d = \frac{1}{T}\int_0^{T/2} V_{out}(t)\,i_{Dn}(t)\,dt + \frac{1}{T}\int_{T/2}^{T}\left(V_{DD} - V_{out}(t)\right)i_{Dp}(t)\,dt$$

where $i_{Dn}(t) = -C_{load}\dfrac{dV_{out}}{dt}$ $\qquad$ $i_{Dp}(t) = C_{load}\dfrac{dV_{out}}{dt}$

$$P_d = \frac{1}{T}\int_0^{T/2} V_{out}(t)\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \frac{1}{T}\int_{T/2}^{T}\left(V_{DD}-V_{out}(t)\right)\left(C_{load}\frac{dV_{out}}{dt}\right)dt$$



$$P_d = \frac{1}{T}\int_{V_{DD}}^{0} -C_{load}V_{out}(t)\,dV_{out} + \frac{1}{T}\int_0^{V_{DD}} C_{load}\left(V_{DD}-V_{out}(t)\right)dV_{out}$$

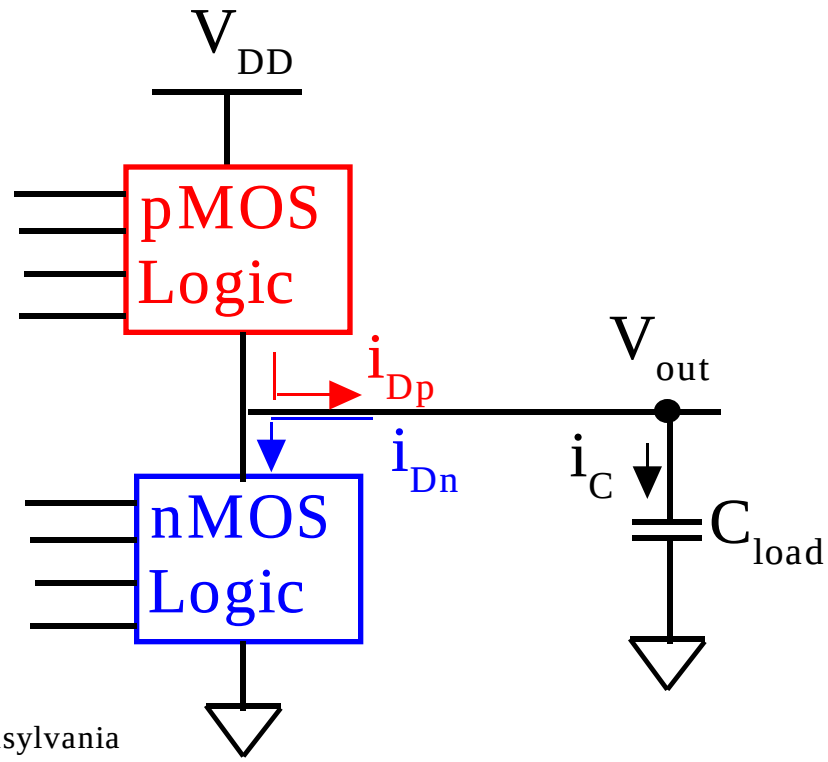
$$= \frac{1}{T}\left[-C_{load}\frac{V_{out}^2}{2}\Big|_{\substack{V_{out}=0\\V_{out}=V_{DD}}} + C_{load}\left(V_{DD}V_{out}-\frac{V_{out}^2}{2}\right)\Big|_{\substack{V_{out}=V_{DD}\\V_{out}=0}}\right]$$

$$P_d = \frac{1}{T}\left[-C_{load}\frac{V_{out}^2}{2}\Big|_{\substack{V_{out}=0\\V_{out}=V_{DD}}} + C_{load}\left(V_{DD}V_{out} - \frac{V_{out}^2}{2}\right)\Big|_{\substack{V_{out}=V_{DD}\\V_{out}=0}}\right]$$

$$= \frac{1}{T}C_{load}V_{DD}^2$$

$$\boxed{P_d = C_{load}V_{DD}^2 f}$$

APPLIES TO GENERAL CMOS LOGIC CIRCUITS



POWER-DELAY PRODUCT

$$PDP = 2P^{*}_{avg}\tau_P = 2\left(C_{load}V_{DD}^{2}f_{max}\right)\tau_P$$

where P^{*}_{avg} = average switching power dissipation at max operating frequency f_{max}.

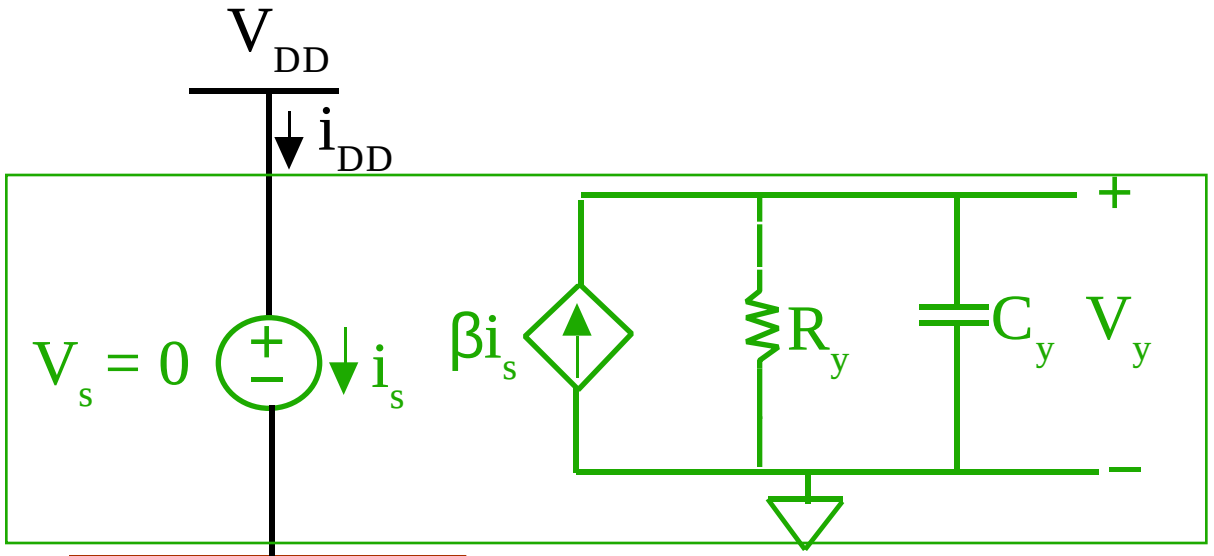
$$f_{max} = \frac{1}{\tau_{PHL} + \tau_{PLH}} \quad \& \quad \tau_P \equiv \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

$$PDP = 2\left(C_{load}V_{DD}^{2}\left(\frac{1}{\tau_{PHL} + \tau_{PLH}}\right)\right)\left(\frac{\tau_{PHL} + \tau_{PLH}}{2}\right) = C_{load}V_{DD}^{2}$$

AVERAGE ENERGY required for a gate to switch its output from LOW to HIGH and from HIGH to LOW

FUNDAMENTAL PARAMETER used to for measuring quality and performance of a CMOS process and gate design

POWER METER SIMULATION



Periodic Input

T = Period

DEVICE or CIRCUIT

C_{load}

$$C_y \frac{dV_y}{dt} = \beta i_S - \frac{V_y}{R_y}$$

IF $R_y C_y >> T$

$$V_y(T) \approx \frac{\beta}{C_y} \int_0^T (1) i_{DD}(\tau) d\tau$$

$$V_y(t) = \frac{\beta}{C_y} \int_0^t e^{-\frac{(t-\tau)}{R_y C_y}} i_{DD}(\tau) d\tau$$

SET $\beta = V_{DD} \frac{C_y}{T}$

$$V_y(T) = V_{DD} \frac{1}{T} \int_0^T i_{DD}(\tau) d\tau \Rightarrow P_d$$