EE 560
MOS TRANSISTOR THEORY
PART 2

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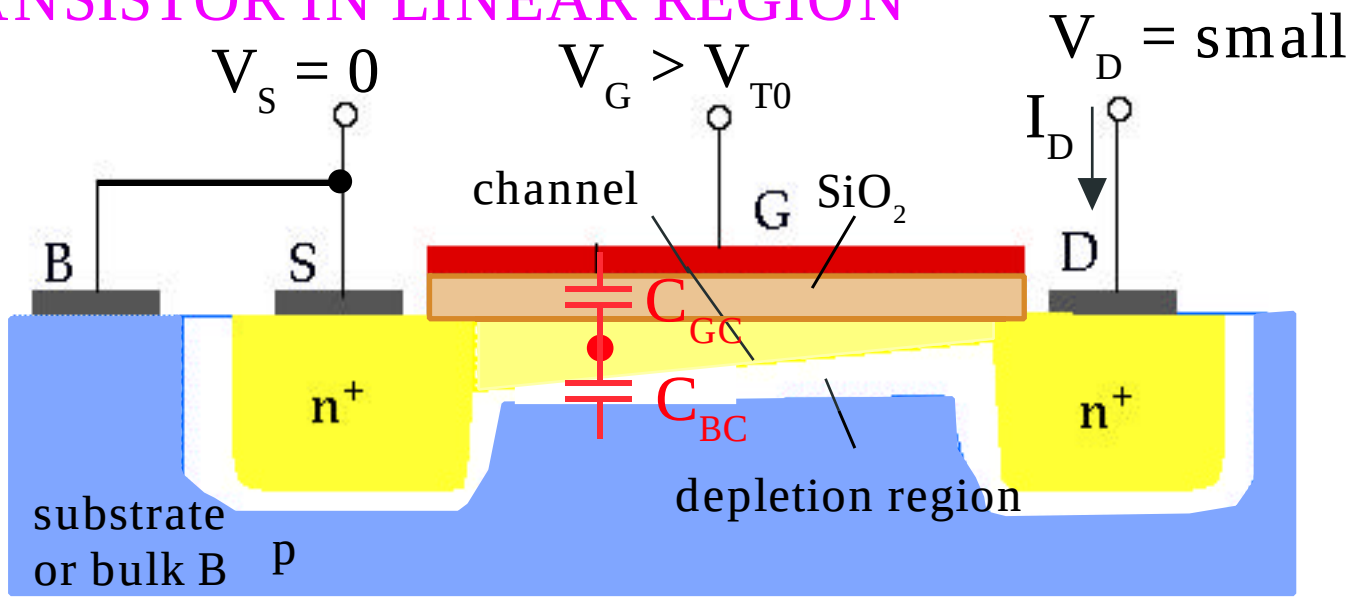
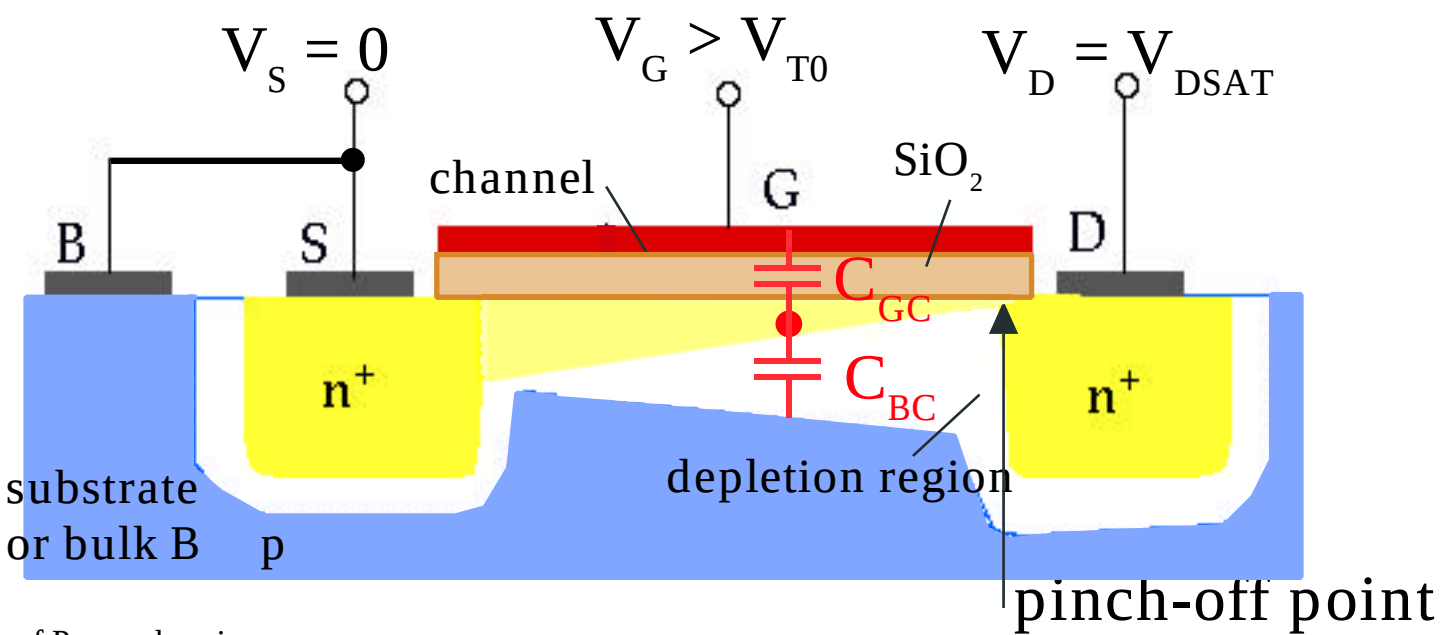
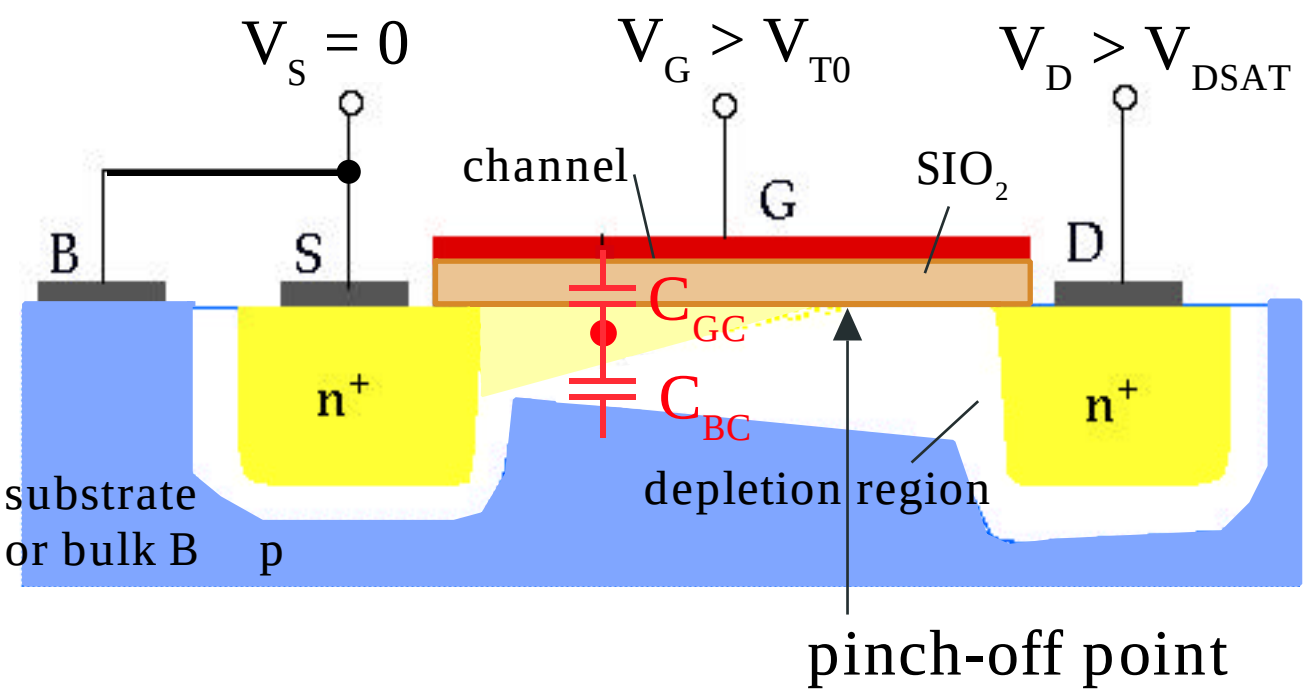
nMOS TRANSISTOR IN LINEAR REGION



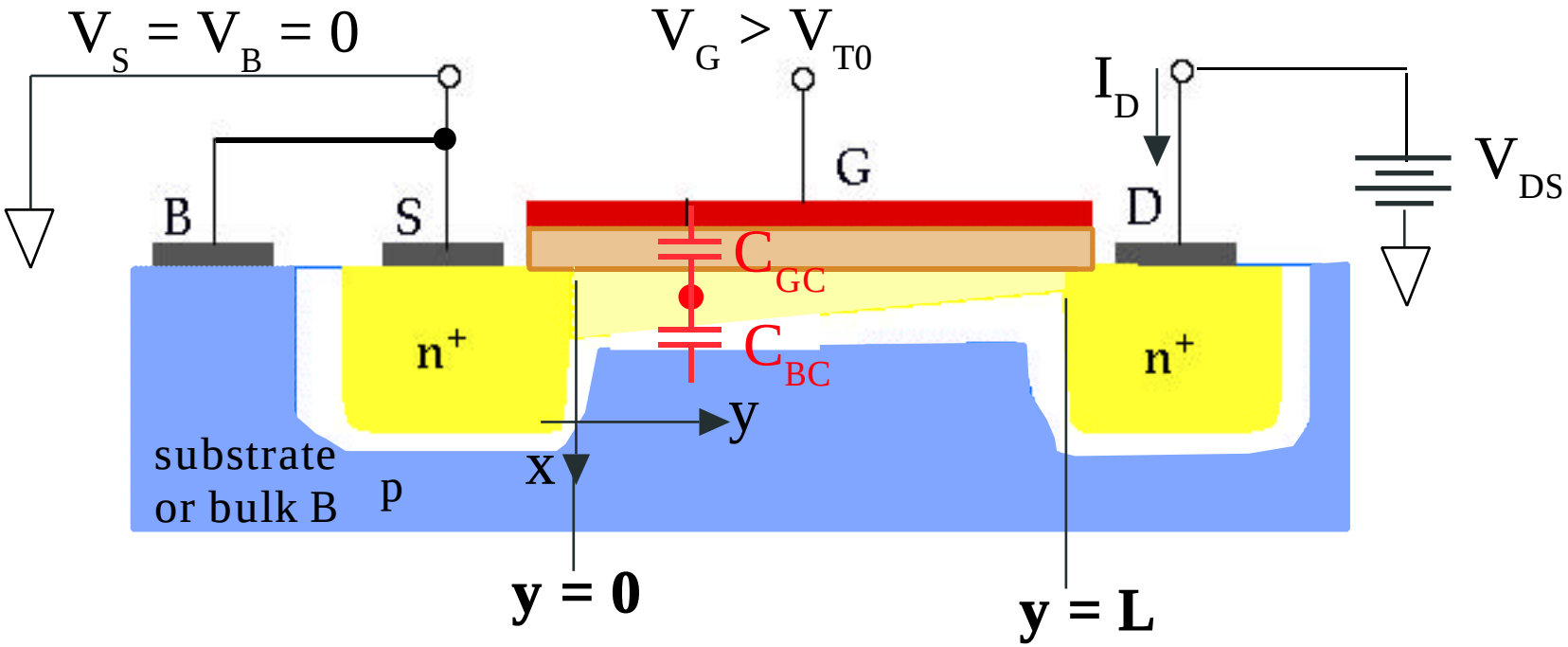
nMOS TRANSISTOR AT EDGE OF SATURATION REGION

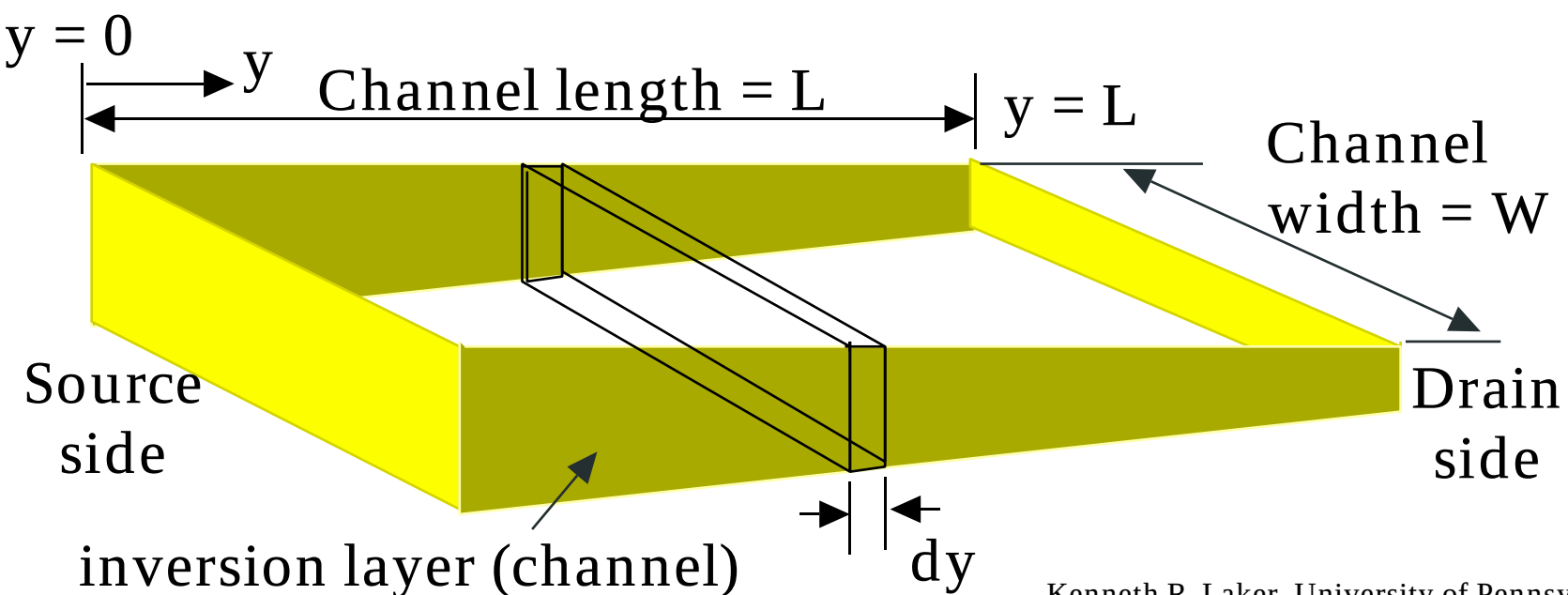


nMOS TRANSISTOR IN SATURATION REGION

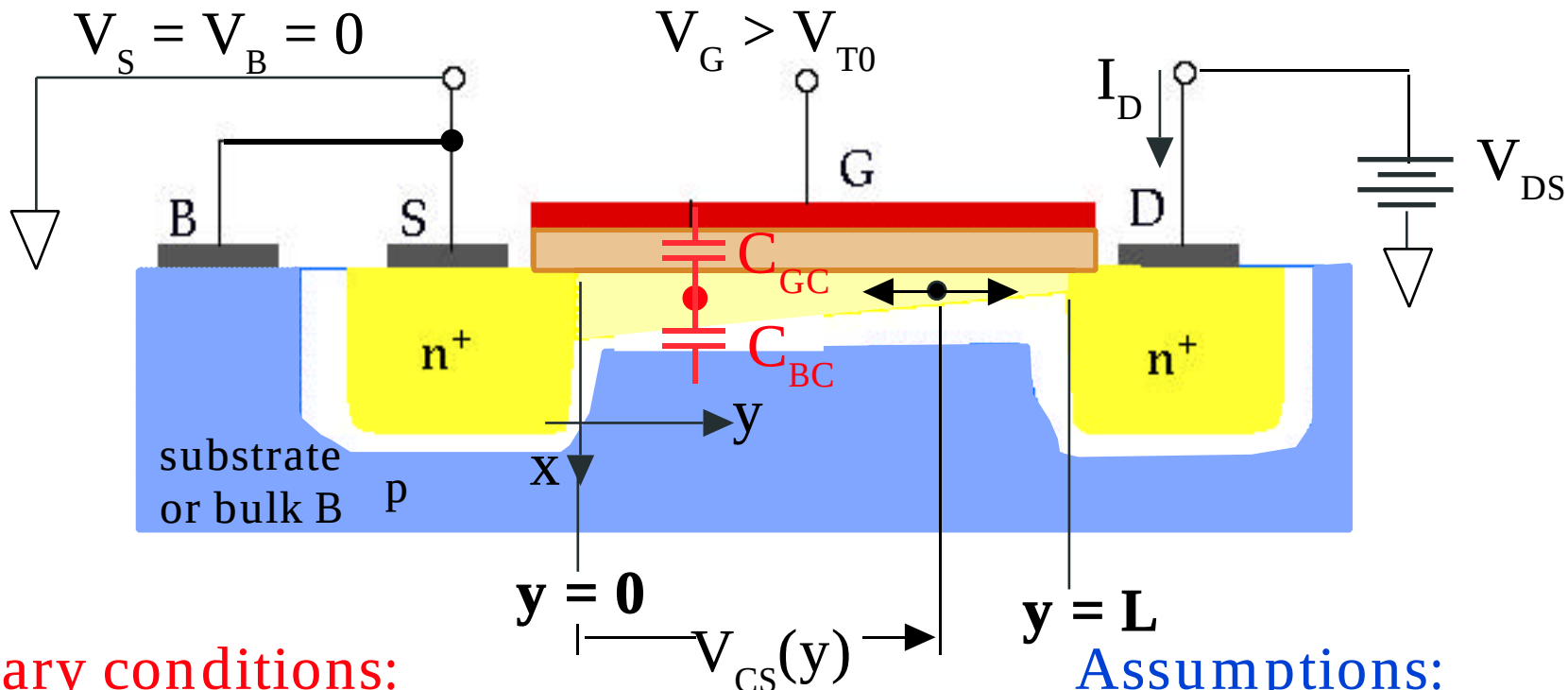


MOSFET CURRENT - VOLTAGE CHARACTERISTICS





MOSFET CURRENT - VOLTAGE CHARACTERISTICS



Boundary conditions:

$$V_{CS}(y = 0) = V_S = 0$$

$$V_{CS}(y = L) = V_{DS}$$

Assumptions:

$$V_{T0}(y) = V_{T0}$$

$$V_{GS} > V_{T0}$$

$$V_{GD} = V_{GS} - V_{DS} > V_{T0}$$

Mobile charge in channel:

$$Q_I(y) = -C_{ox}[V_{GS} - V_{CS}(y) - V_{T0}]$$

$$\mu_n Q_I(y) = \left(\frac{cm^2}{V \cdot s}\right)\left(\frac{c}{cm^2}\right) = \frac{c/s}{V} = \frac{I}{V}$$

$$dR = -\frac{dy}{W}\left(\frac{1}{\mu_n Q_I(y)}\right)$$

μ_n = electron mobility
= $cm^2/Vsec$
[μ –> U0 in SPICE]

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

Boundary conditions:

$$V_{CS}(y=0) = V_S = 0$$

$$V_{CS}(y=L) = V_{DS}$$

$$Q_I(y) = -C_{ox}[V_{GS} - V_{CS}(y) - V_{T0}]$$

$$dR = -\frac{dy}{W}\left(\frac{1}{\mu_n Q_I(y)}\right)$$

$$dV_{CS} = I_D dR = -\frac{I_D}{W\mu_n Q_I(y)}dy$$

Integrating along the channel $0 \le y \le L$ and $0 \le V_{CS} < V_{DS}$:

$$\int_0^L I_D dy = -W\mu_n \int_0^{V_{DS}} Q_I(y)\,dV_{CS}$$

i.e.

$$\int_0^L I_D y = W\mu_n C_{ox} \int_0^{V_{DS}} [V_{GS} - V_{CS} - V_{T0}]\,dV_{CS}$$

$$I_y\Big|_{y=0}^{y=L} = W\mu_n C_{ox}\left[(V_{GS} - V_{T0})V_{CS} - V_{CS}^2/2\right]\Big|_{V_{CS}=0}^{V_{CS}=V_{DS}}$$

$$= W\mu_n C_{ox}[(V_{GS} - V_{T0})V_{DS} - V_{DS}^2/2]$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2]$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2]$$

$$= \frac{k'}{2}\frac{W}{L}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2]$$

$$k' = \mu_n C_{ox}$$

[k' -> KP in SPICE]

$$= \frac{k}{2}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2]$$

$$k = k'\frac{W}{L}$$

EXAMPLE 3.4

For an n-MOS transistor with $\mu_n = 600\ cm^2/Vsec$, $C_{ox} = 7 \times 10^{-8}\ F/cm^2$ $W = 20\ \mu m$, $L = 2\ \mu m$, $V_{T0} = 1.0\ V$, plot the relationship between I_D and V_{DS}, V_{GS}.

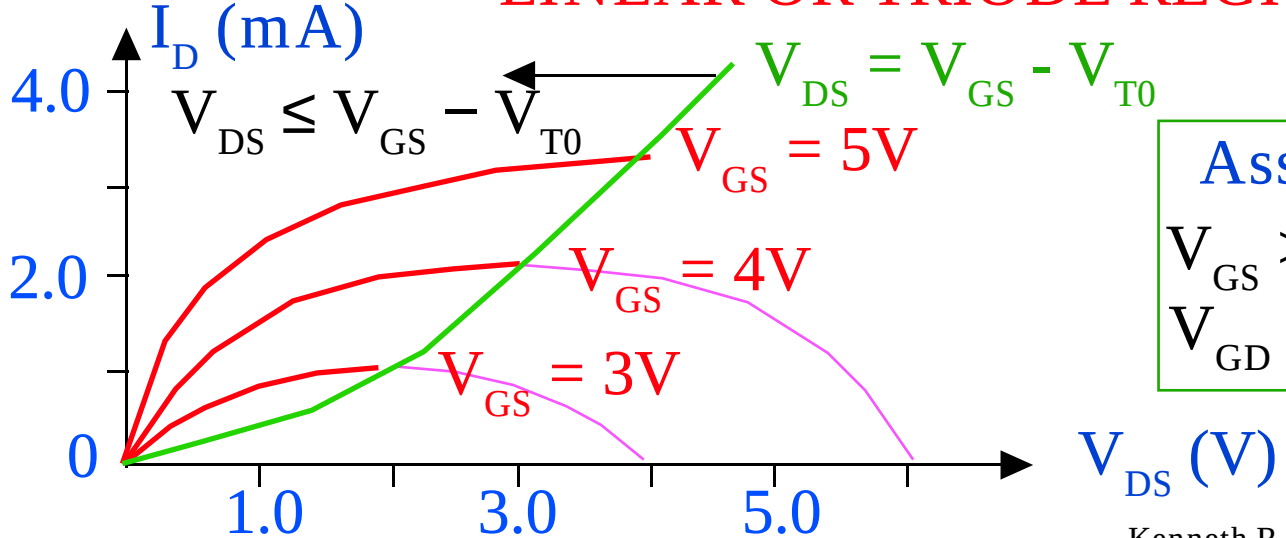
$$I_D = \frac{k}{2}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2] \quad \text{where} \quad k = \mu_n C_{ox} \frac{W}{L}$$

F = C / V

$$k = \mu_n C_{ox} \frac{W}{L} = (600\,cm^2/Vsec)(7 \times 10^{-8}\,F/cm^2)\frac{20\mu m}{2\mu m} = 0.42\,mA/V^2$$

$$I_D = 0.21 mA/V^2[2(V_{GS} - 1.0)V_{DS} - V_{DS}^2]$$

LINEAR OR TRIODE REGION



Assumptions:

$V_{GS} > V_{T0}$

$V_{GD} = V_{GS} - V_{DS} > V_{T0}$

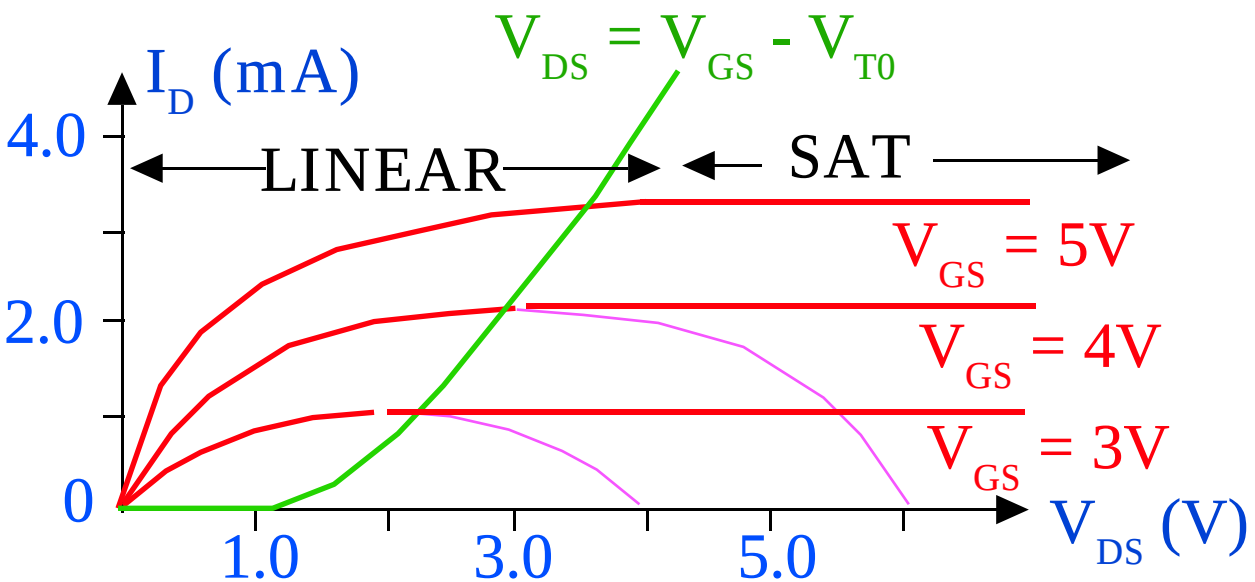
MOSFET CURRENT - VOLTAGE CHARACTERISTICS

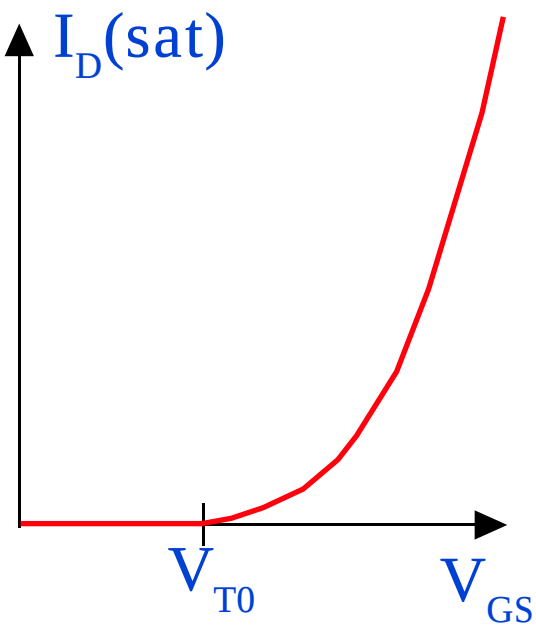
$V_{DS} \geq V_{GS} - V_{T0} = V_{DSAT}$ SATURATION REGION

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2] \Big|_{@V_{DS}=V_{DSAT}=V_{GS}-V_{T0}}$$

$$= \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_{T0})(V_{GS}-V_{T0})-(V_{GS}-V_{T0})^2]$$

$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{T0})^2$$





CHANNEL LENGTH MODULATION

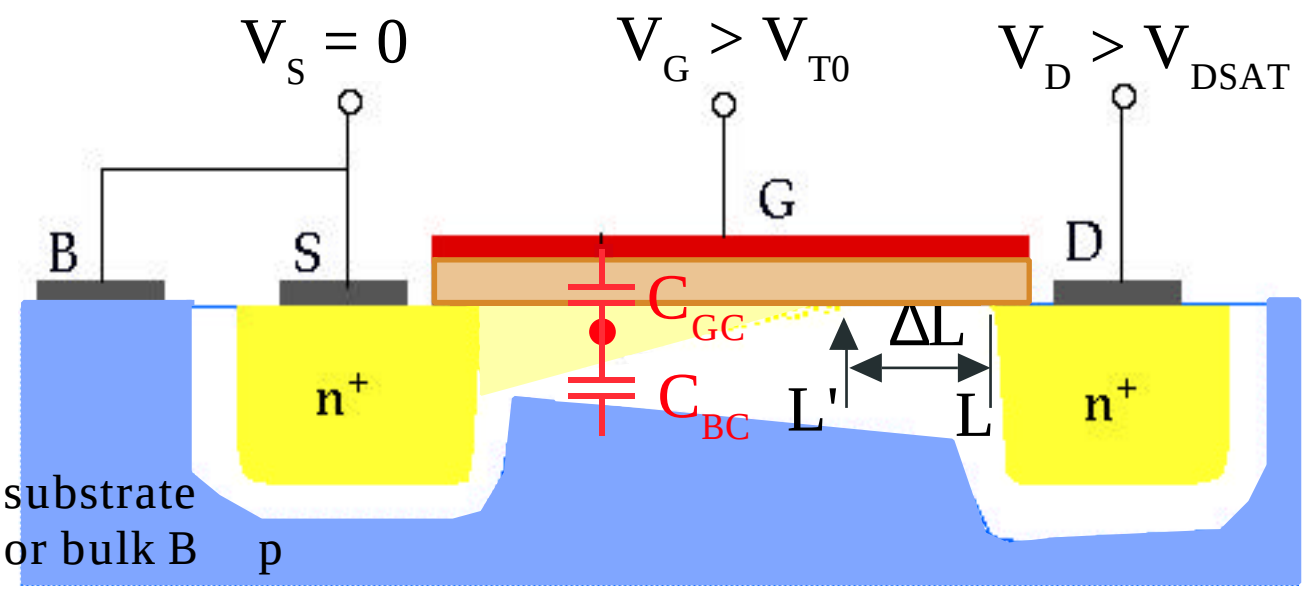
Boundary conditions:

$$V_{CS}(y=0) = V_S = 0 \rightarrow Q_I(y=0) = -C_{ox}[V_{GS} - V_{T0}]$$

$$V_{CS}(y=L) = V_{DS} \rightarrow Q_1(y=L) = -C_{ox}[V_{GS} - V_{DS} - V_{T0}]$$

$$Q_I(y) = -C_{ox}[V_{GS} - V_{CS}(y) - V_{T0}]$$

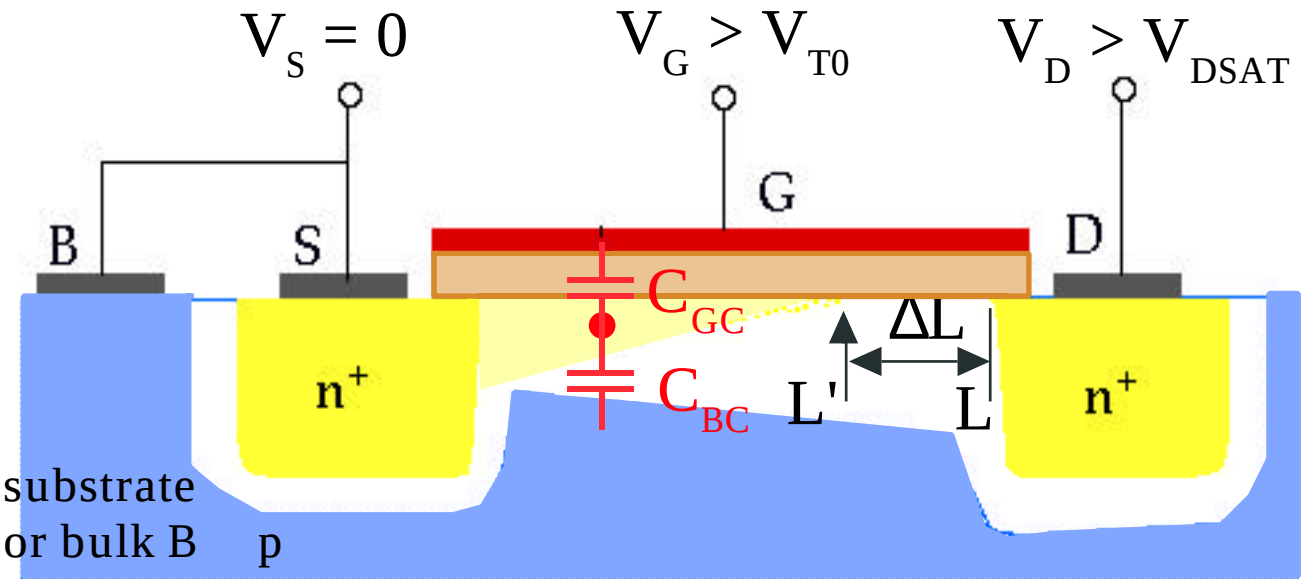
$= 0 \; @ \; V_{DS} = V_{DSAT}$



$L' = L - \Delta L$ effective channel length

$$V_{CS}(y = L') = V_{DSAT}$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS



$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L'}(V_{GS} - V_{T0})^2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L(1-\frac{\Delta L}{L})}(V_{GS} - V_{T0})^2$$

where $\Delta L \quad \sqrt{V_{DS} - V_{DSAT}}$

emperical relation: $\frac{1}{1-\frac{\Delta L}{L}} = 1 + \lambda V_{DS}$ [λ -> LAMBDA in SPICE]

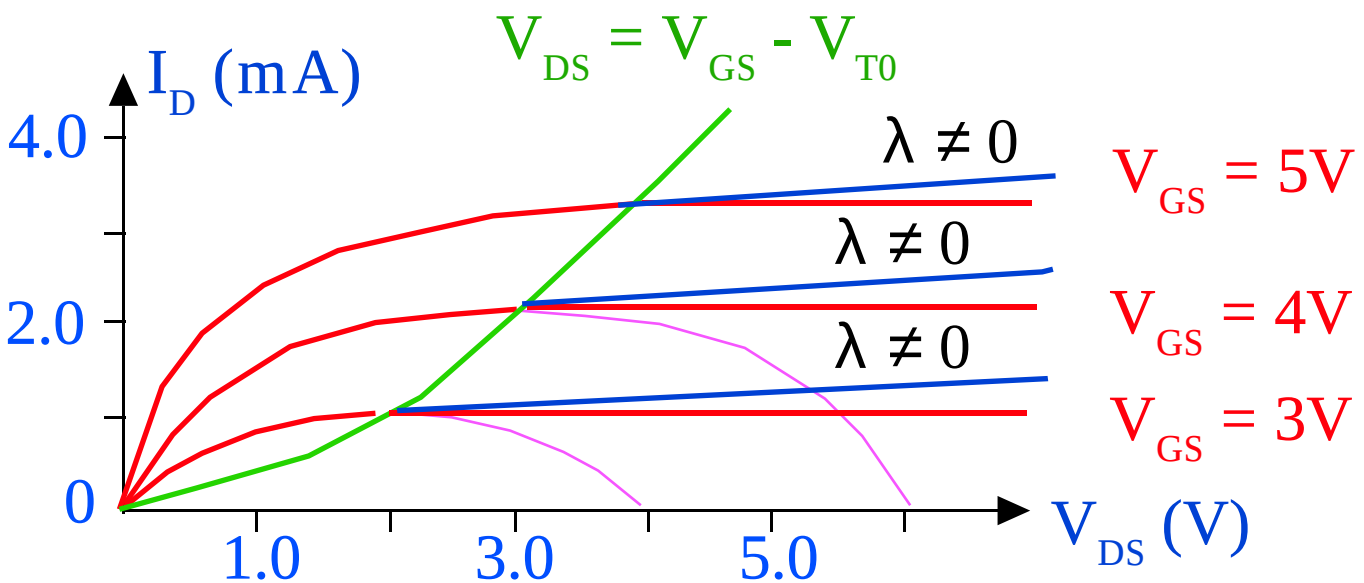
λ = channel length modulation coefficent (V^{-1})

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L'}(V_{GS} - V_{T0})^2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L(1-\frac{\Delta L}{L})}(V_{GS} - V_{T0})^2$$

$$\frac{1}{1-\frac{\Delta L}{L}} = 1 + \lambda V_{DS}$$

$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$



SUBSTRATE BIAS EFFECT

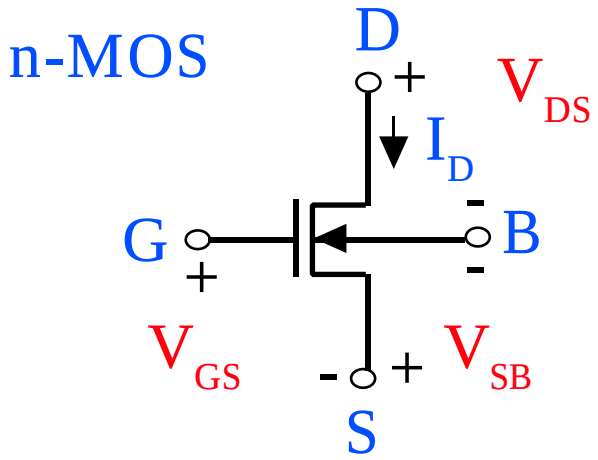
$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

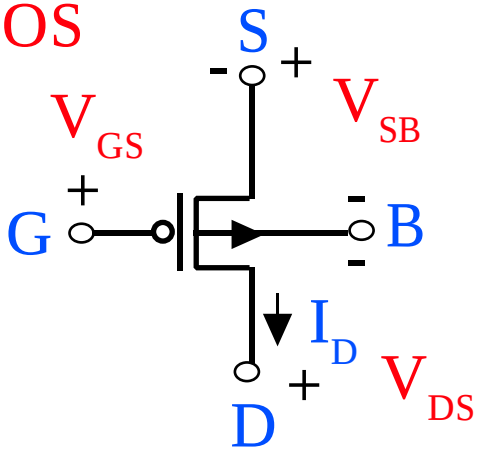
$$I_D(\text{lin}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_T(V_{SB}))V_{DS} - V_{DS}^2\right]$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T(V_{SB}))^2(1 + \lambda V_{DS})$$

$$I_D = f(V_{GS}, V_{DS}, V_{SB})$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS





n-MOS $I_D = 0$ for $V_{GS} \le V_T$

$$I_D(\text{lin}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_T(V_{SB}))V_{DS} - V_{DS}^2\right] \quad V_{GS} > V_T,\ V_{DS} < V_{GS} - V_T$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T(V_{SB}))^2(1 + \lambda V_{DS}) \quad V_{GS} > V_T,\ V_{DS} \ge V_{GS} - V_T$$

p-MOS $I_D = 0$ for $V_{GS} \ge V_T$

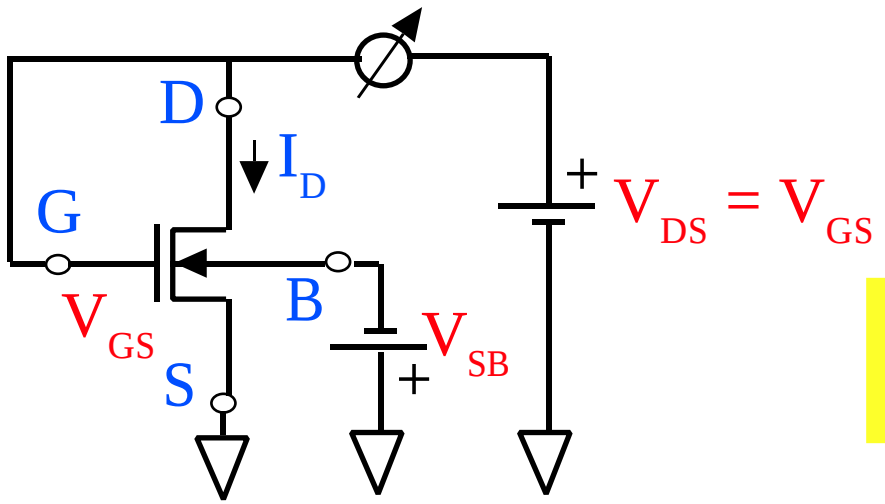
$$I_D(\text{lin}) = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_T(V_{SB}))V_{DS} - V_{DS}^2\right] \quad V_{GS} < V_T,\ V_{DS} > V_{GS} - V_T$$

$$I_D(\text{sat}) = \frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T(V_{SB}))^2(1 + \lambda V_{DS}) \quad V_{GS} < V_T,\ V_{DS} \le V_{GS} - V_T$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

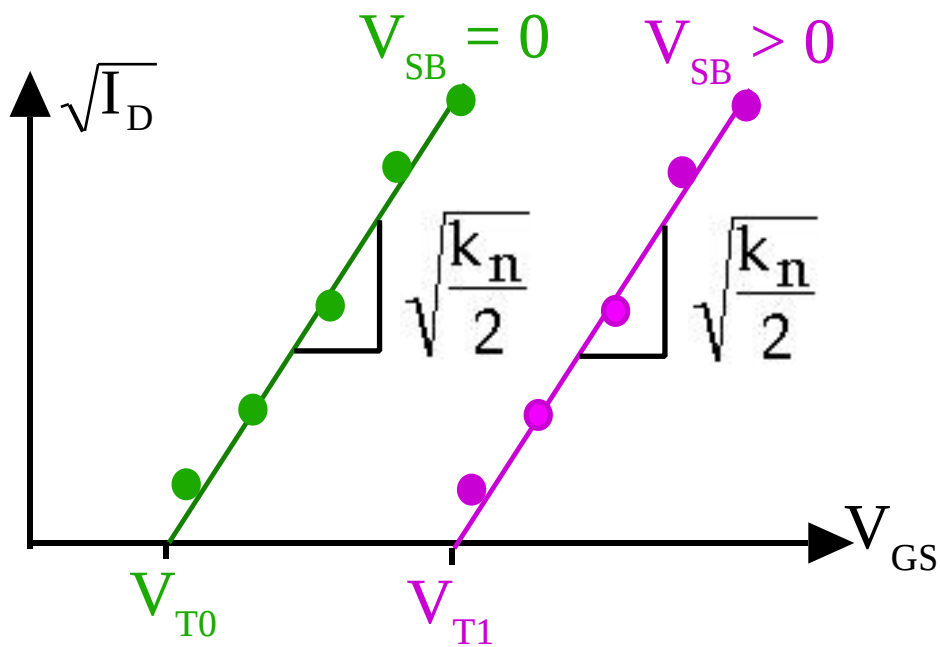
MEASUREMENT OF PARAMETERS (V_{T0}, γ, λ, k_n, k_p)

$$k_n = \mu_n C_{ox} \frac{W}{L} \qquad k_p = \mu_p C_{ox} \frac{W}{L}$$



$$I_D(sat) = \frac{k_n}{2}(V_{GS} - V_{T0})^2$$

$$\sqrt{I_D(sat)} = \sqrt{\frac{k_n}{2}}(V_{GS} - V_{T0})$$



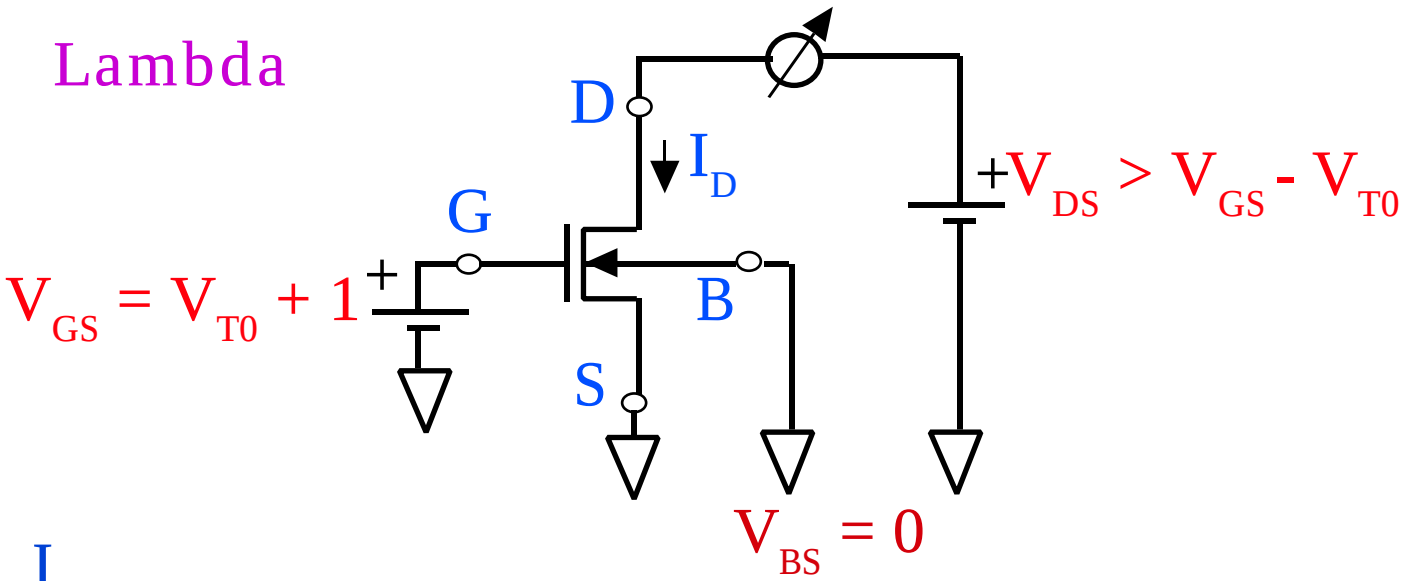
Gamma

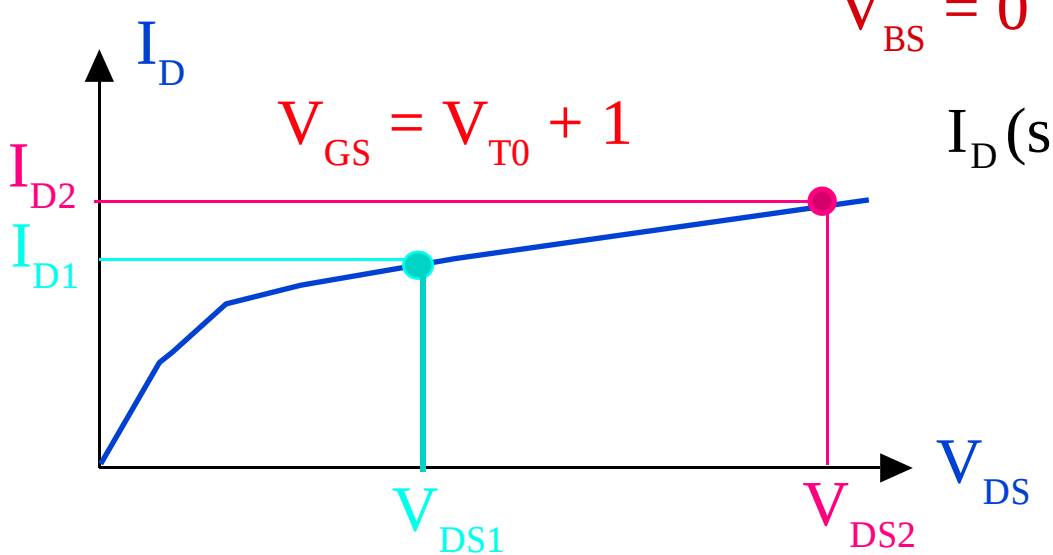
$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}}$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

Lambda



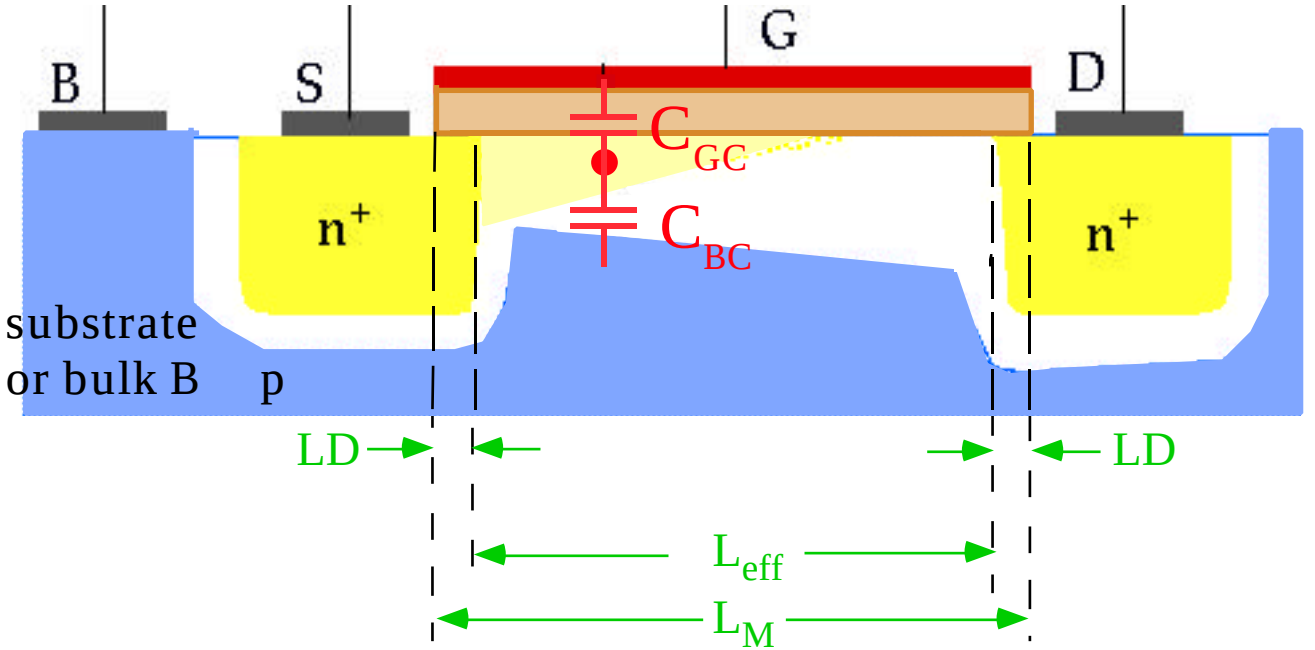


$$I_D(sat) = k_n(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

$V_{GS} = V_{T0} + 1$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

EFFECTIVE CHANNEL LENGTH AND WIDTH



SPICE Parameters

$L_{eff} = L_M - 2LD - DL$

LD -> under diffusion

DL -> error in photolith and etch

$W_{eff} = W_M - DW$

SPICE Parameters

DW -> error in photolith and etch

MOSFET - SCALING

SCALING -> refers to ordered reduction in dimensions of the MOSFET and other VLSI features

- Reduce Size of VLSI chips.
- Change operational charateristics of MOSFETs and parasitics.
- Phyiscal limits restrict degree of scaling that can be achieved.

SCALING FACTOR = $\alpha > 1$ --> S

First-order "constant field" MOS scaling theory:

The electric field E is kept constant, and the scaled device is obtained by applying a dimensionless scale-factor α to (such that E is unchanged):

a. All dimensions, including those vertical to the surface $(1/\alpha)$

b. device voltages $(1/\alpha)$

c. the concentration densities (α).

$(1/\alpha)/(1/\alpha) = 1$ $\qquad$ $\alpha(1/\alpha) = 1$

$$E_{ox} = V_{GS} / t_{ox} \quad <=> \quad dE = -\frac{q}{\varepsilon} N_A dx$$

MOSFET - SCALING

Alternative Scaling Rules:

Constant Voltage Scaling, i.e. V_{DD} is kept constant, while the process is scaled.

a. All dimensions, including those vertical to the surface $(1/\alpha)$

b. device voltages (1)

c. the concentration densities (α^2).

$1/(1/\alpha) = \alpha$ $\qquad$ $\alpha^2(1/\alpha) = \alpha$

$$E_{ox} = V_{GS} / t_{ox} \quad <=> \quad dE = -\frac{q}{\varepsilon} N_A dx$$

Lateral Scaling: only the gate length is scaled $L = 1/\alpha$ (gate-shrink).

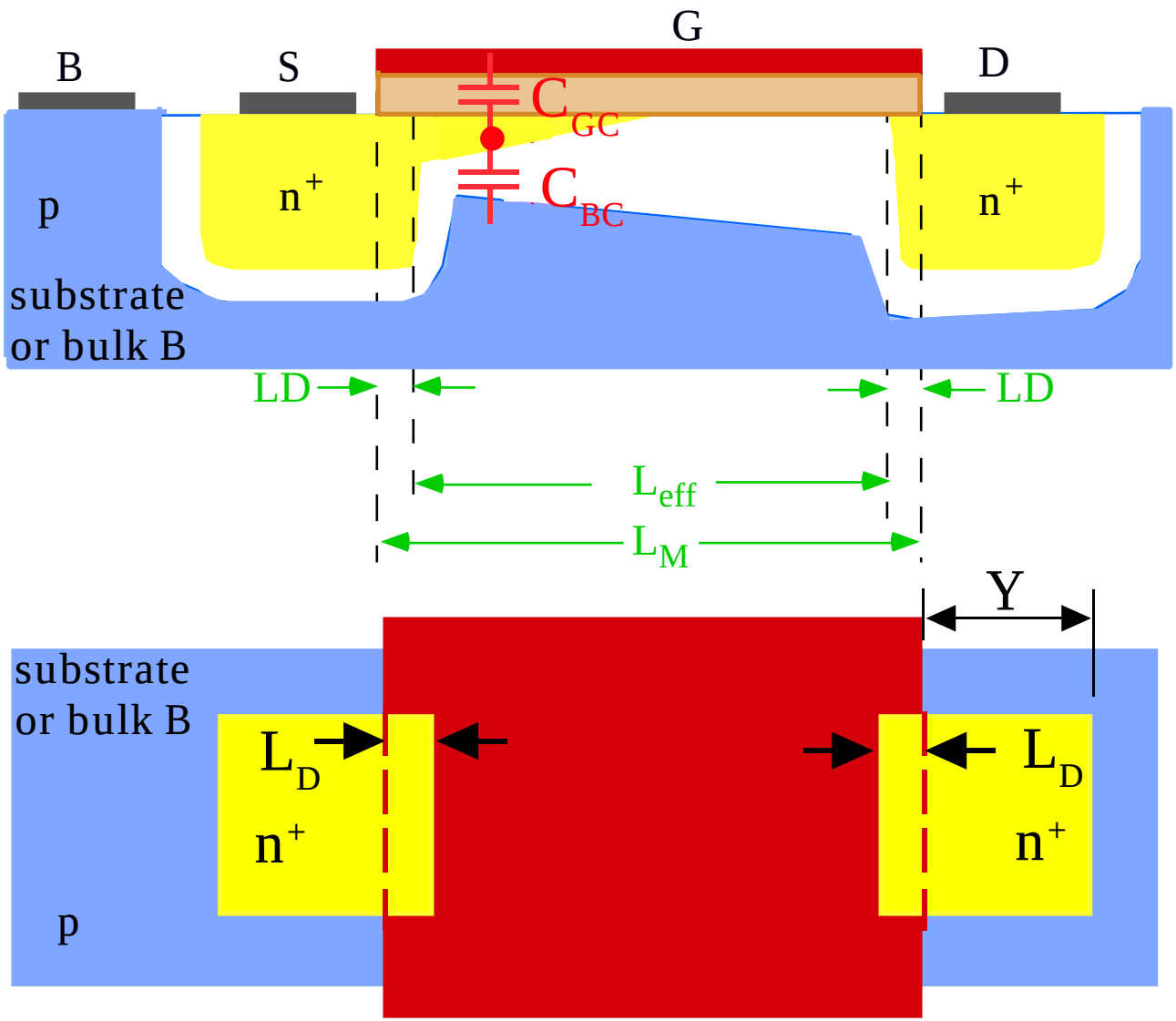
Year	1980	1983	1985	1987	1989	1991	1993	1995
Feature Size(μm)	5.0	3.5	2.5	1.75	1.25	1.0	0.8	0.6

Historical reduction in min feature size for typical CMOS Process

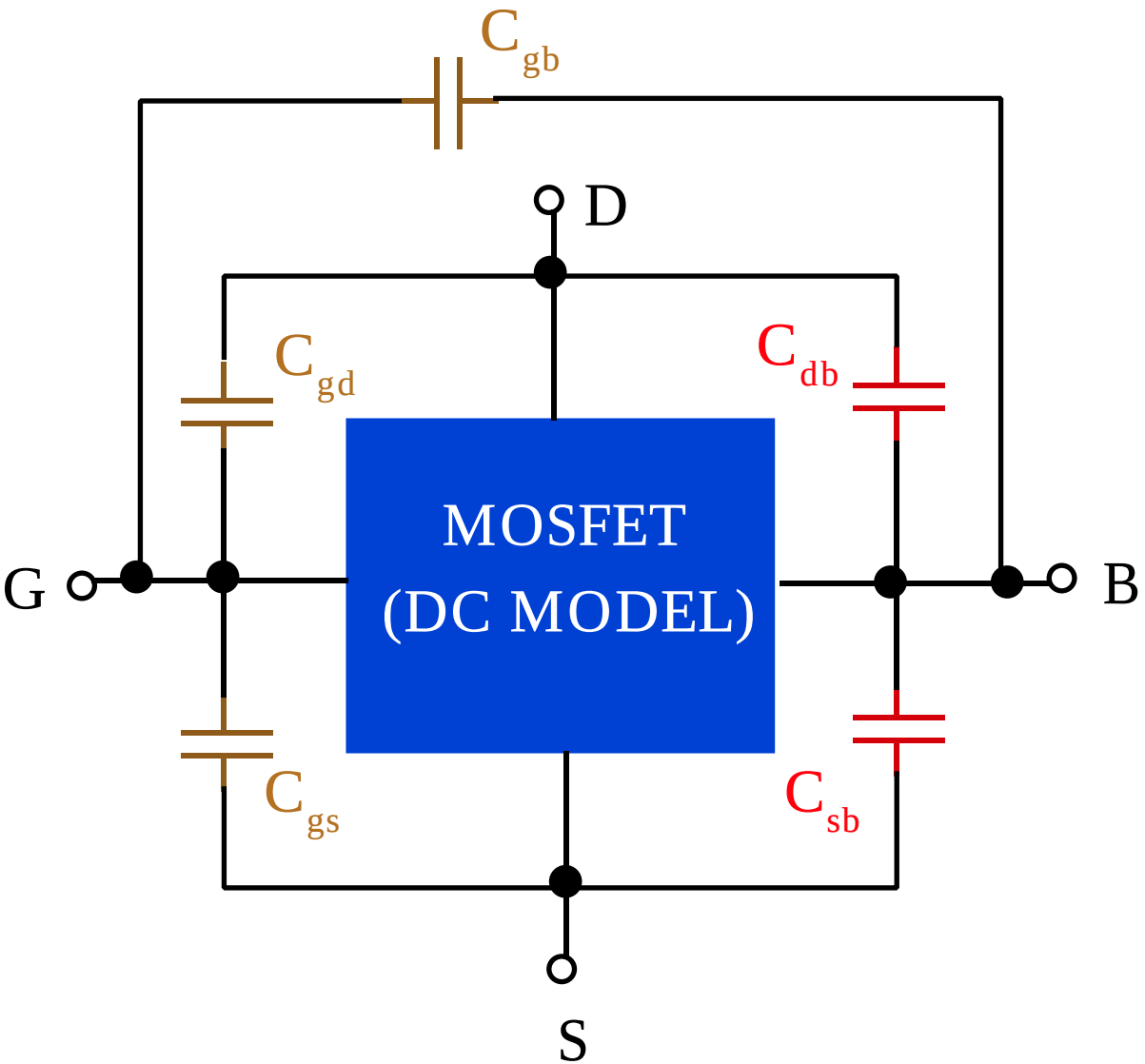
Influence of Scaling on MOS Device Performance

PARAMETER	SCALING MODEL		
	Constant Field	Constant Voltage	Lateral
Length (L)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Width (W)	$1/\alpha$	$1/\alpha$	1
Supply Voltage (V)	$1/\alpha$	1	1
Gate Oxide thickness (t_{ox})	$1/\alpha$	$1/\alpha$	1
Junction depth (X_j)	$1/\alpha$	$1/\alpha$	1
Substrate Doping (N_A)	α	α^2	1
Current (I) - $(W/L)\,(1/t_{ox})V^2$	$1/\alpha$	α	α
Power Dissipation (P) - IV	$1/\alpha^2$	α	α
Electric Field Across Gate Oxide - V/t_{ox}	1	α	1
Load Capacitance (C) - $WL\,(1/t_{ox})$	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate Delay (T) - VC/I	$1/\alpha$	$1/\alpha^2$	$1/\alpha^2$

MOSFET CAPACITANCES



MOSFET CAPACITANCES



C_{gd}, C_{gs}, C_{gb} -> Oxide Capacitances

C_{db}, C_{sb} -> Junction Capacitances

MOSFET CAPACITANCES

OXIDE Capacitances $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

a. Overlap Caps

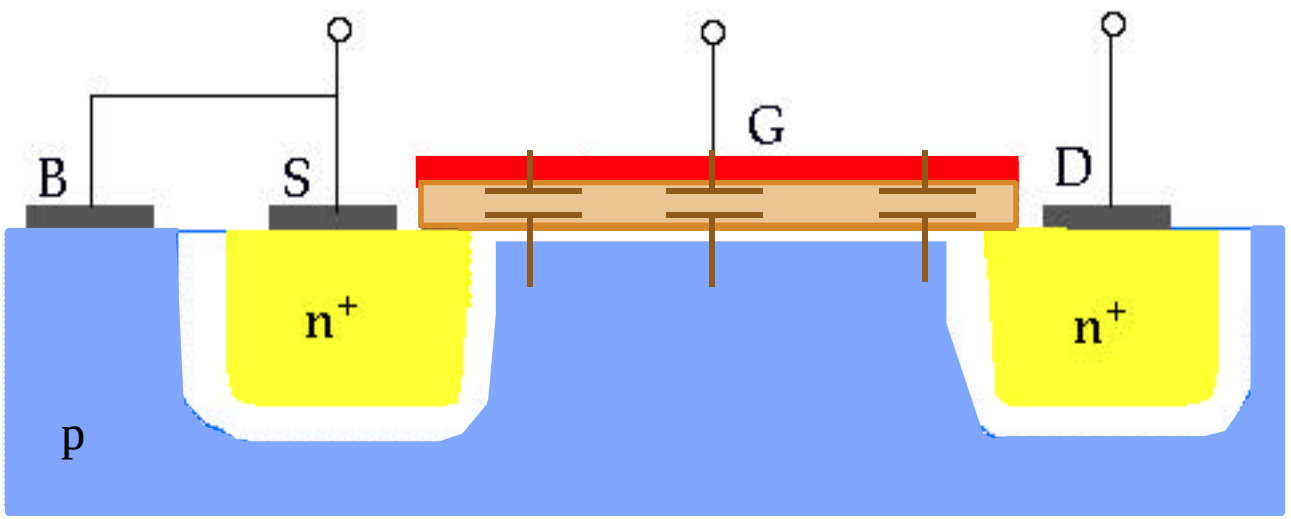
$C_{GS}(overlap) = C_{ox}\, W\, L_D$

$C_{GD}(overlap) = C_{ox}\, W\, L_D$

ALL MOSFET OPERATION REGIONS

b. Gate - Channel

MOSFET - Cut-off Region



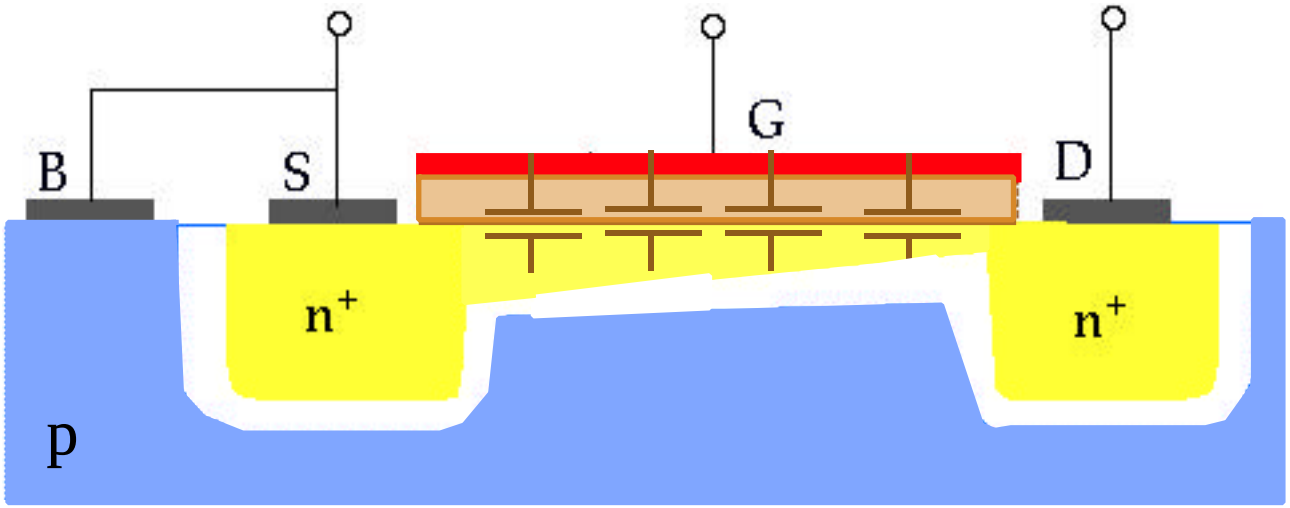
$C_{gb} = C_{ox}\, W\, L$

$C_{gs} = C_{gd} = 0$

MOSFET CAPACITANCES

b. Gate - Channel

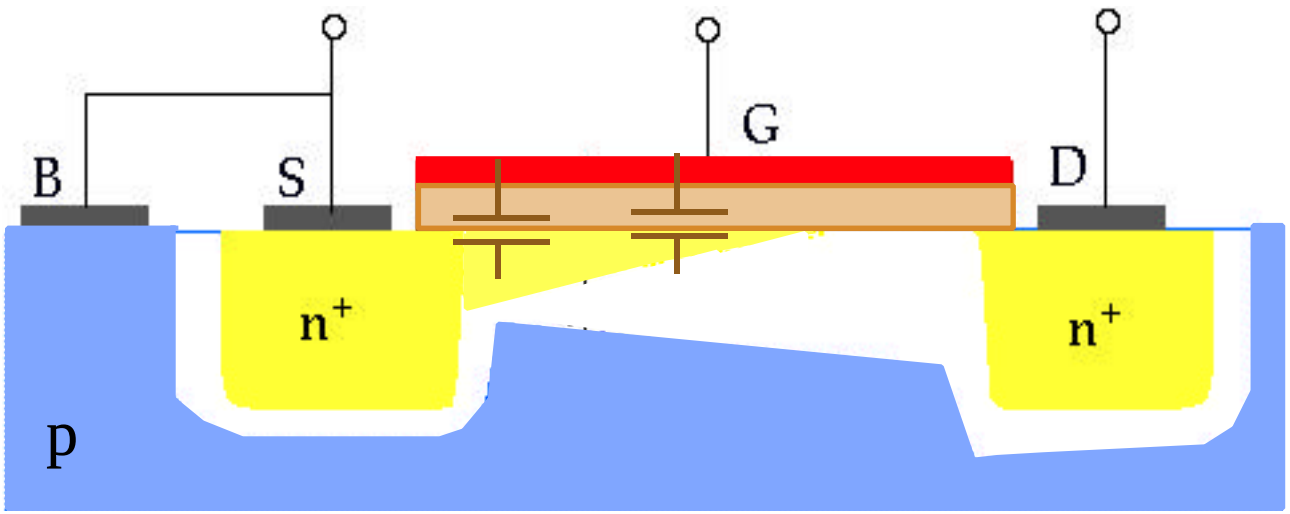
MOSFET - Linear Region



$$C_{gb} = 0$$

$$C_{gs} = (1/2)\, C_{ox}\, W\, L$$

$$C_{gd} = (1/2)\, C_{ox}\, W\, L$$

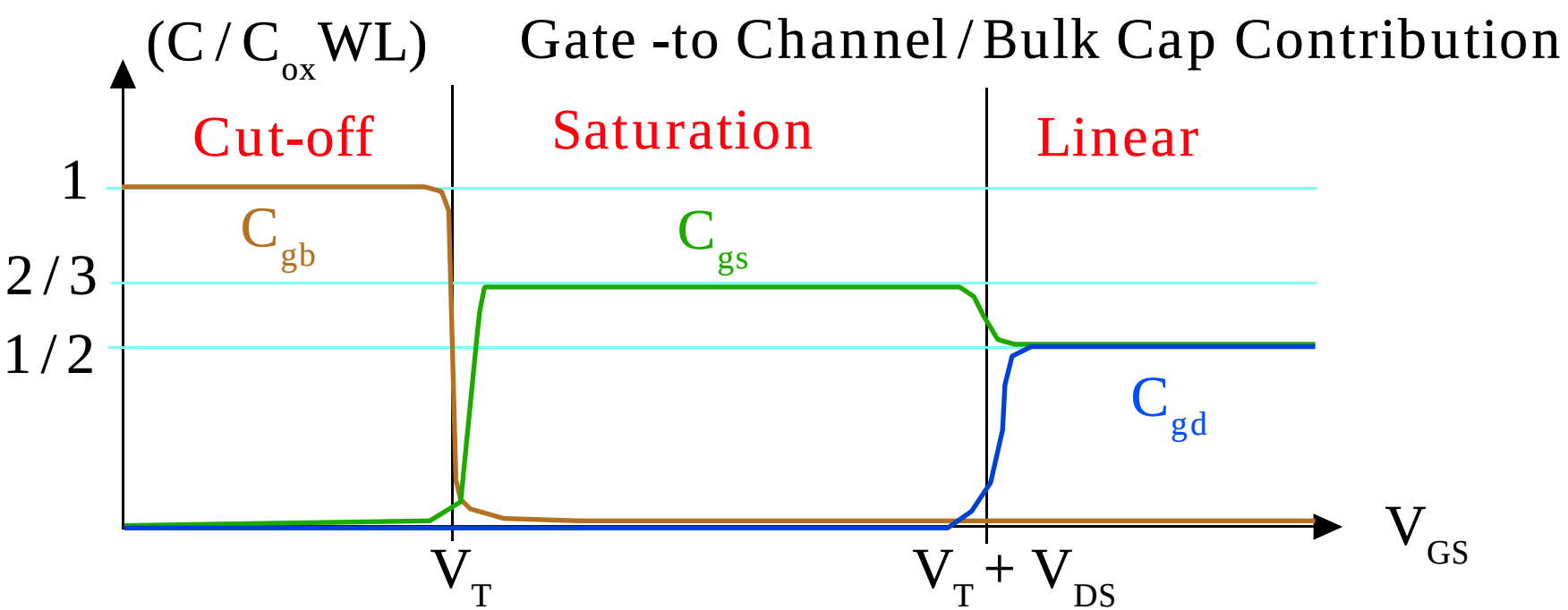


$$C_{gb} = 0$$

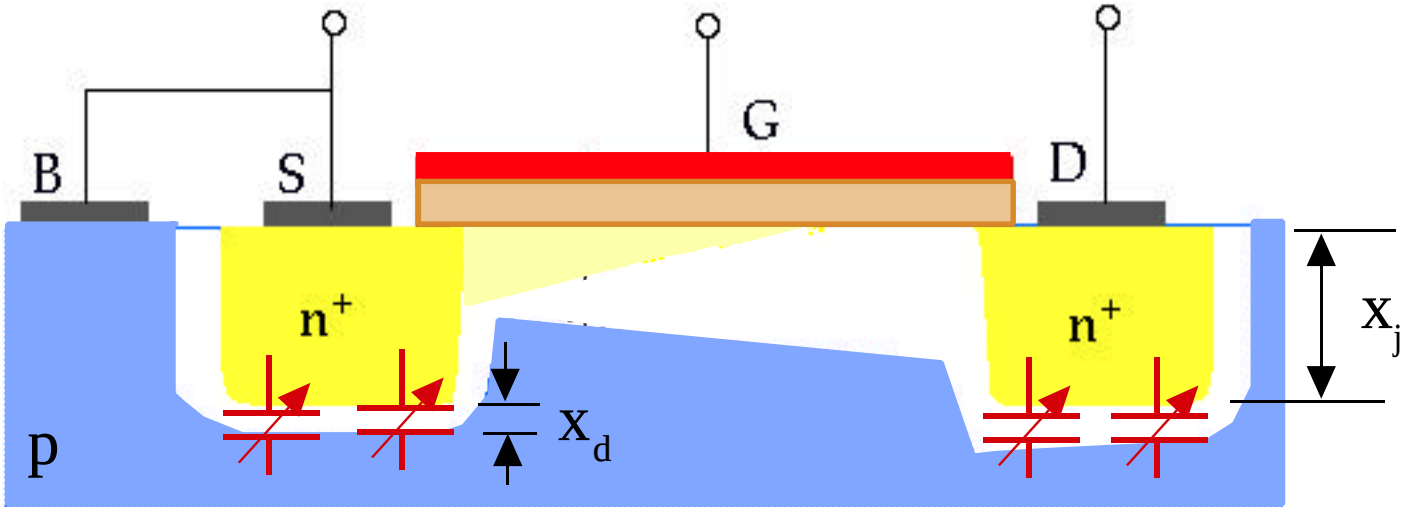
$$C_{gs} = (2/3)\, C_{ox}\, W\, L$$

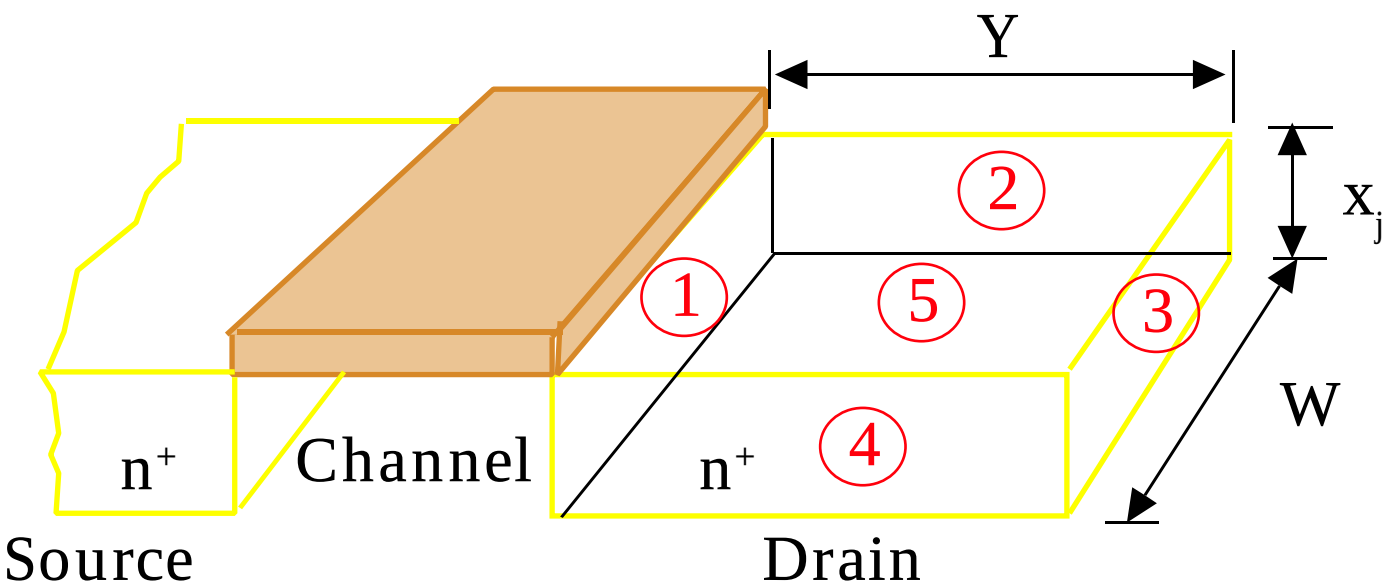
$$C_{gd} = 0$$

Capacitance	Cut-off	Linear	Saturation
C_{gb}(total)	$C_{ox}WL$	0	0
C_{gd}(total)	0 + $C_{ox}WL_D$	$0.5C_{ox}WL$ + $C_{ox}WL_D$	0 + $C_{ox}WL_D$
C_{gs}(total)	0 + $C_{ox}WL_D$	$0.5C_{ox}WL$ + $C_{ox}WL_D$	$(2/3)C_{ox}WL$ + $C_{ox}WL_D$

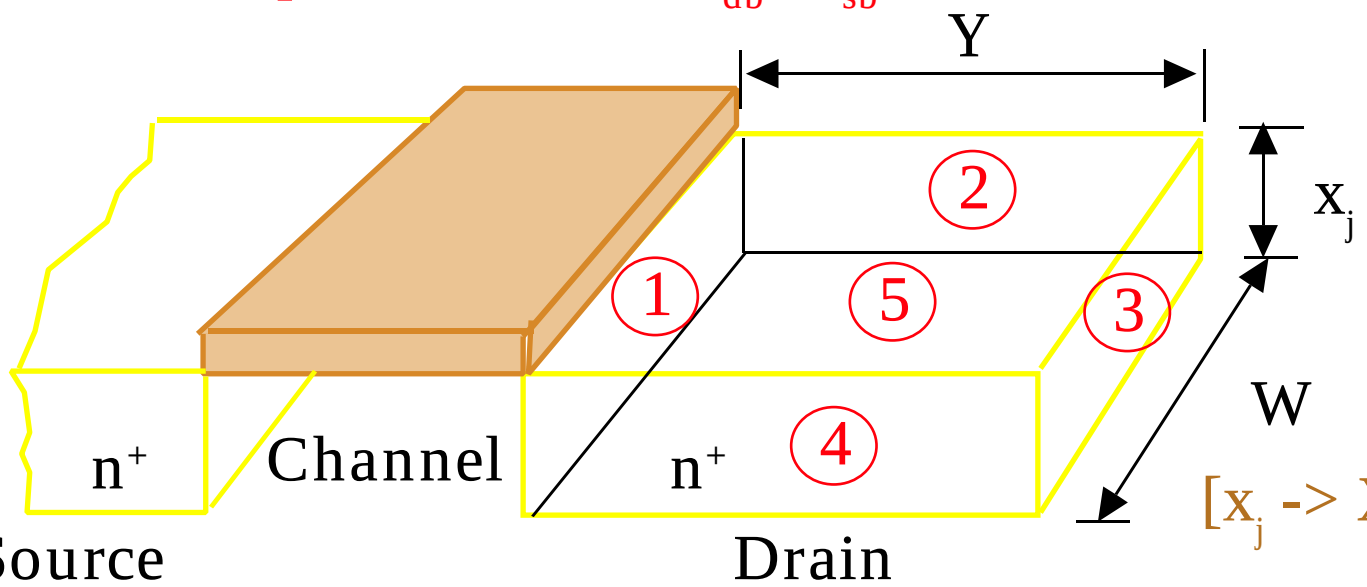


JUNCTION Capacitances -> C_{db}, C_{sb}





JUNCTION Capacitances -> C_{db}, C_{sb}



[x_j -> XJ in SPICE]

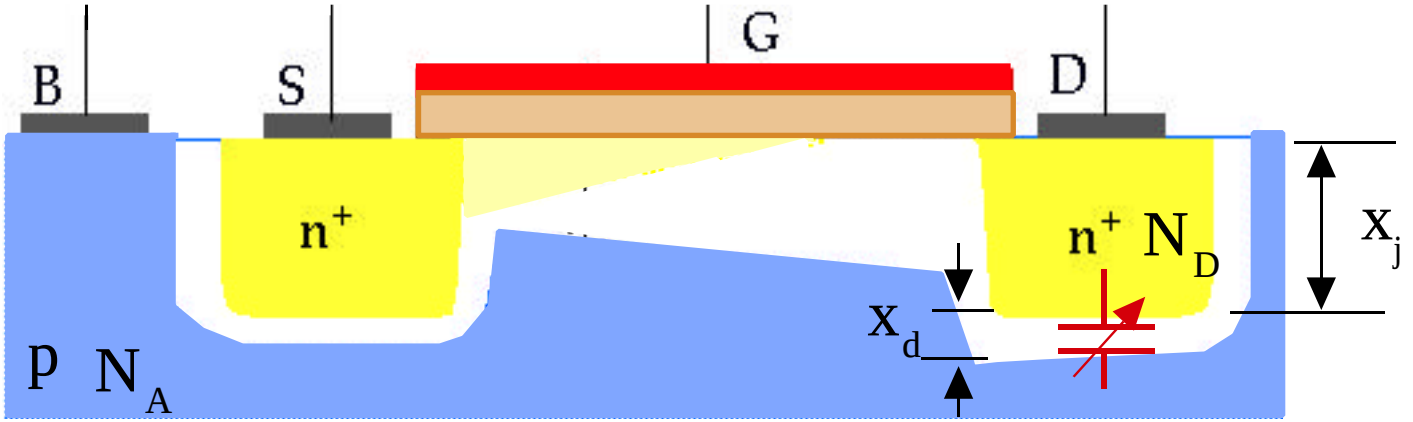
Junction	Area	Type
1	W x_j	n^+ / p
2	Y x_j	n^+ / p^+
3	W x_j	n^+ / p^+
4	Y x_j	n^+ / p^+
5	WY	n^+ / p

p - Substrate -> N_A

p^+ - Channel-stop -> $10N_A$

JUNCTION Capacitances -> C_{db}, C_{sb}

n^+, p junctions



$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(\varphi_0 - V)}$$

$\leftrightarrow$ V = Ext bias --> V_{DB}, V_{SB}

$$\varphi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

built-in junction potential

[φ_0 -> PB in SPICE]

Depletion-region charge

$$Q_j = Aq\left(\frac{N_A N_D}{N_A + N_D}\right)x_d = A\sqrt{2\varepsilon_{Si}\, q\left(\frac{N_A N_D}{N_A + N_D}\right)(\varphi_0 - V)}$$

A = junction area

$$C_j = \left|\frac{dQ_j}{dV}\right| = A\sqrt{\frac{\varepsilon_{Si}\, q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)}\frac{1}{\sqrt{\varphi_0 - V}} = \frac{AC_{j0}}{\left(1 - \frac{V}{\varphi_0}\right)^{1/2}}$$

[AS, AD -> Source, Drain Areas in SPICE]

$$C_j = \left|\frac{dQ_j}{dV}\right| = A\sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)}\frac{1}{\sqrt{\varphi_0 - V}} = \frac{AC_{j0}}{\left(1 - \frac{V}{\varphi_0}\right)^{1/2}} \quad (F)$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\frac{1}{\varphi_0}} \quad (F/cm^2)$$

$C_j = C_{j0}$ when $V = 0$

m = grading coefficent

m = 1/2 for abrubt junction

[m = MJ in SPICE]

[C_{j0} -> CJ in SPICE]

[φ_0 -> PB in SPICE]

EQUIVALENT LARGE SIGNAL CAPACTIANCE

$$C_{eq} = \frac{\Delta Q_j}{\Delta V} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1} = \frac{1}{V_2 - V_1}\int_{V_1}^{V_2} C_j(V)dV$$

$$= \frac{AC_{j0}\varphi_0(-1)}{(V_2 - V_1)(1-m)}\left[\left(1 - \frac{V_2}{\varphi_0}\right)^{1-m} - \left(1 - \frac{V_1}{\varphi_0}\right)^{1-m}\right] \quad m = 1/2$$

$$C_{eq} = AC_{j0}K_{eq} \qquad 0 < K_{eq} < 1 \text{ --> Voltage Equiv Factor}$$

n^+, p^+ junctions (Sidewalls)

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A(sw) N_D}{N_A(sw) + N_D}\right)\frac{1}{\varphi_{0sw}}} \qquad (F/cm^2)$$

Since all sidewalls have depth = x_j: [x_j -> XJ in SPICE]

$$C_{jsw} = C_{j0sw}\, x_j \qquad (F/cm)$$

[C_{jsw} -> CJSW in SPICE]

EQUIVALENT LARGE SIGNAL CAPACTIANCE

$$C_{eq}(sw) = P\, C_{jsw}\, K_{eq}(sw)$$

P = sidewall perimeter

[PS, PD -> Source, Drain Perimeters in SPICE]

$$K_{eq}(sw) = -\frac{2\varphi_{0sw}}{(V_2 - V_1)}\left[\left(1 - \frac{V_2}{\varphi_{0sw}}\right)^{1/2} - \left(1 - \frac{V_1}{\varphi_{0sw}}\right)^{1/2}\right] \qquad m(sw) = 1/2$$

[m(sw) -> MJSW in SPICE]

EXAMPLE 3-8

Determine the total junction capacitance at the drain, i.e. C_{db}, for the n-channel enhancement MOSFET in Fig. 1. The process parameters are

Substrate doping	$N_A = 2 \times 10^{15}$ cm^{-3}
Source / drain (n+) doping	$N_D = 10^{20}$ cm^{-3}
Sidewall (p+) doping	$N_A(sw) = 4 \times 10^{16}$ cm^{-3}
Gate oxide thickness	$t_{ox} = 45$ nm
Junction depth	$x_j = 1.0$ µm

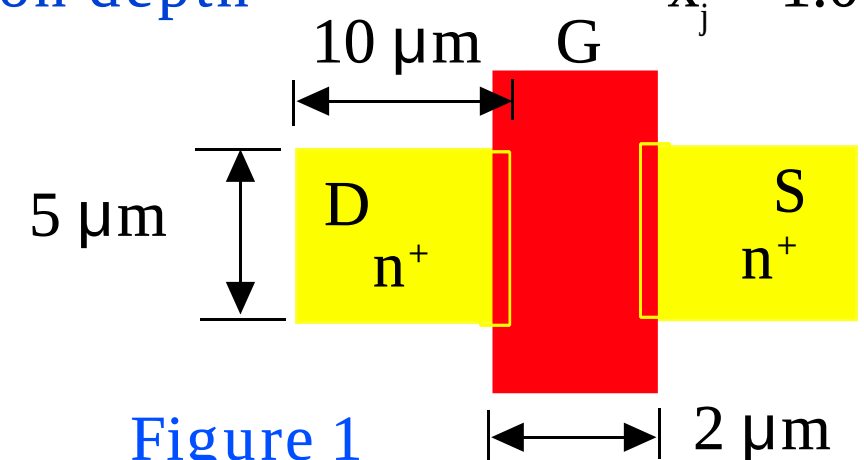


Figure 1

Source, Drain are surrounded by p^+ channel-stop. The substrate is biased at 0V. Assume the drain voltage range is 0.5 V to 5.0 V.

$$C_{db} = C_{eq} + C_{eq}(sw)$$
$$= A_D C_{j0} K_{eq} + P_D C_{j0sw} x_j K_{eq}(sw)$$

where

$A_D C_{j0} K_{eq}$

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\frac{1}{\phi_0}}$$

$$K_{eq} = -\frac{2\phi_0}{(V_{BD2} - V_{BD1})}\left[\left(1 - \frac{V_{BD2}}{\phi_0}\right)^{1/2} - \left(1 - \frac{V_{BD1}}{\phi_0}\right)^{1/2}\right]$$

$P_D C_{j0sw} x_j K_{eq}(sw)$

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A(sw) N_D}{N_A(sw) + N_D}\right)\frac{1}{\phi_{0sw}}}$$

$$K_{eq}(sw) = -\frac{2\phi_{0sw}}{(V_{BD2} - V_{BD1})}\left[\left(1 - \frac{V_{BD2}}{\phi_{0sw}}\right)^{1/2} - \left(1 - \frac{V_{BD1}}{\phi_{0sw}}\right)^{1/2}\right]$$

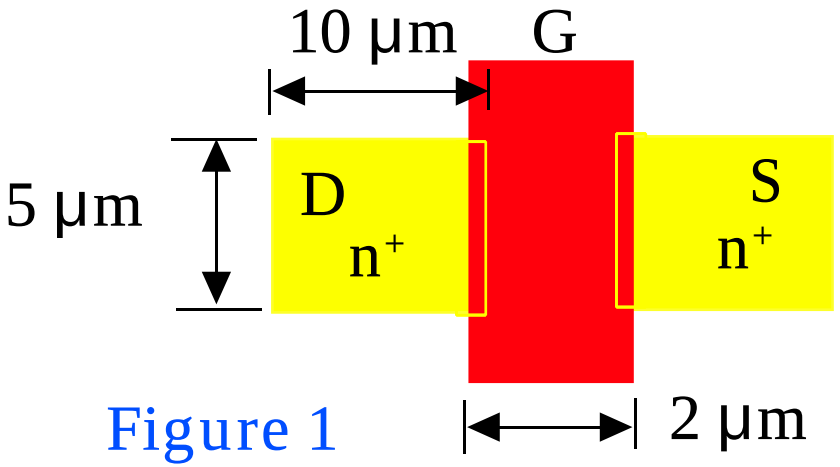


Figure 1

$N_A = 2 \times 10^{15}\ cm^{-3}$
$N_D = 10^{20}\ cm^{-3}$
$N_A(sw) = 4 \times 10^{16}\ cm^{-3}$
$t_{ox} = 45\ nm$
$x_j = 1.0\ \mu m$

φ_0, φ_{0sw}

$$\varphi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026\,V \ln\left(\frac{(2\times10^{15})10^{20}}{2.1\times10^{20}}\right) = 0.896\,V$$

$$\varphi_{0sw} = \frac{kT}{q}\ln\left(\frac{N_A(sw) N_D}{n_i^2}\right) = 0.026\,V \ln\left(\frac{(4\times10^{16})10^{20}}{2.1\times10^{20}}\right) = 0.975\,V$$

C_{j0}, C_{j0sw}

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si}\, q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\frac{1}{\varphi_0}}$$

$$= \sqrt{\frac{(1.04\times10^{-12}\,F/cm)(1.6\times10^{-19}\,C)}{2}\left(\frac{(2\times10^{15})10^{20}}{2\times10^{15}+10^{20}}\right)\frac{1}{0.896V}}$$

$$= 1.35\times10^{-8}\,F/cm^2$$

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A(sw) N_D}{N_A(sw) + N_D}\right)\frac{1}{\phi_{0sw}}}$$

$$= \sqrt{\frac{(1.04 \times 10^{-12}\ F/cm)(1.6 \times 10^{-19}\ C)}{2}\left(\frac{(4 \times 10^{16})10^{20}}{4 \times 10^{16} + 10^{20}}\right)\frac{1}{0.975V}}$$

$$= 5.83 \times 10^{-8}\ F/cm^2$$

C_{jsw}

$$C_{jsw} = C_{j0sw}\, x_j = (5.83 \times 10^{-8}\ F/cm^2)(10^{-4}\ cm) = 5.83 pF/cm$$

K_{eq}, $K_{eq}(sw)$ $\quad V_{BD1} = V_B - V_{D1} = 0 - 0.5V = -0.5V$

$$V_{BD2} = V_B - V_{D2} = 0 - 5V = -5V$$

$$K_{eq} = -\frac{2\phi_0}{(V_{BD2} - V_{BD1})}\left[\left(1 - \frac{V_{BD2}}{\phi_0}\right)^{1/2} - \left(1 - \frac{V_{BD1}}{\phi_0}\right)^{1/2}\right]$$

$$= -\frac{2(0.896V)}{(-5V - (-0.5V))}\left[\left(1 - \frac{-5V}{0.896V}\right)^{1/2} - \left(1 - \frac{-0.5V}{0.896V}\right)^{1/2}\right] = 0.52$$

$$K_{eq}(sw) = -\frac{2(0.975V)}{(-5V-(-0.5V))}\left[\left(1-\frac{-5}{0.975V}\right)^{1/2}-\left(1-\frac{-0.5}{0.975V}\right)^{1/2}\right] = 0.53 \approx K_{eq}$$

Area, Perimeter

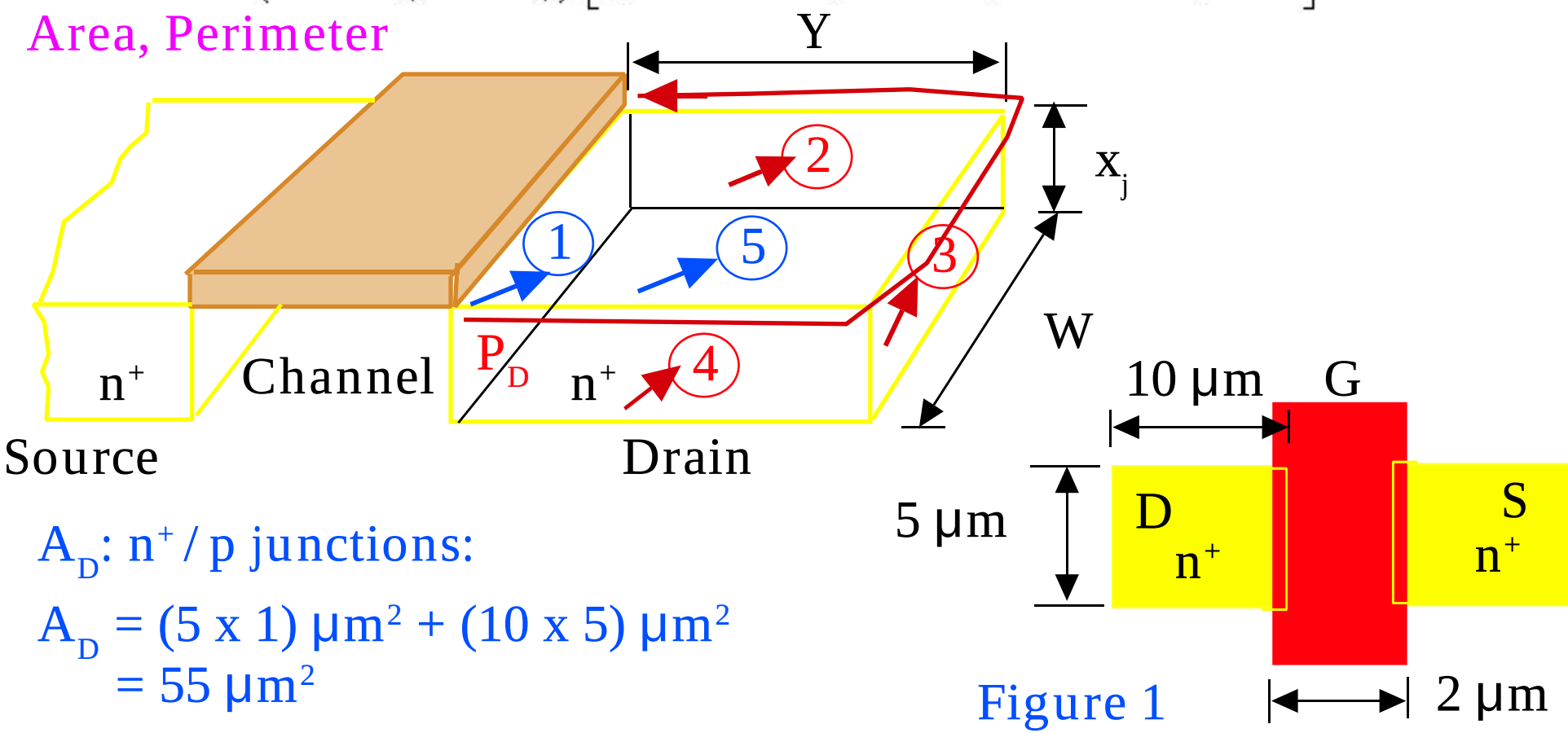


Figure 1

A_D: n^+ / p junctions:

$A_D = (5 \times 1)\ \mu m^2 + (10 \times 5)\ \mu m^2$
$= 55\ \mu m^2$

P_D: n^+ / p^++ junctions:

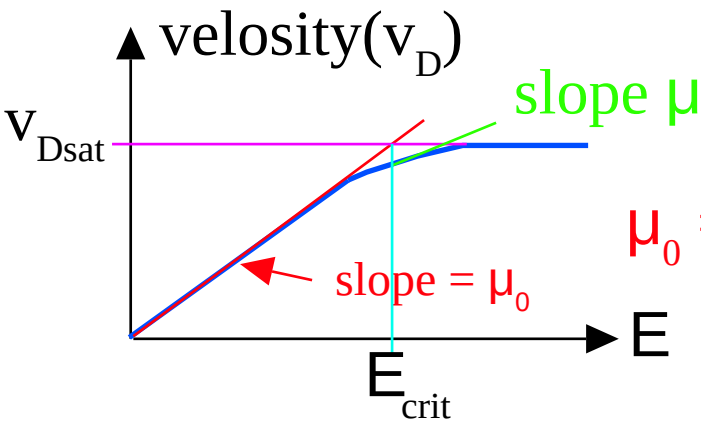
$P_D = 2Y + W = 20\ \mu m + 5\ \mu m = 25\ \mu m$

$$C_{db} = A_D C_{j0} K_{eq} + P_D C_{j0sw} K_{eq}(sw) = 11.6\,fF$$

Mobility Degradation due to Longitudinal Electric Field:

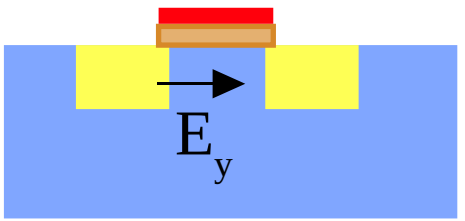
VELOSITY SATURATION

(very small channel lengths + high supply voltages)



Note $\mu_s < \mu_0$

$\mu_0 = v_{sat}/E_{crit}$



[SPICE Parameters: U0 -> μ_0, UCRIT -> E_{crit}, VMAX -> v_{sat}]

$$I_D(sat) = W\, v_{DSAT}\, |Q_I|$$

$$= W\, v_{DSAT}\, C_{ox}\, V_{DSAT}$$

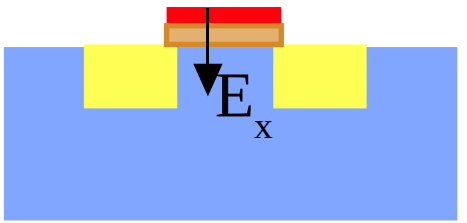
$$= W\, v_{DSAT}\, C_{ox}\, (V_{GS} - V_T)$$

Note: $I_D(sat)$ = linear f($V_{GS} - V_T$), independent of L

Mobility Degradation due to Tranverse Electric Field:

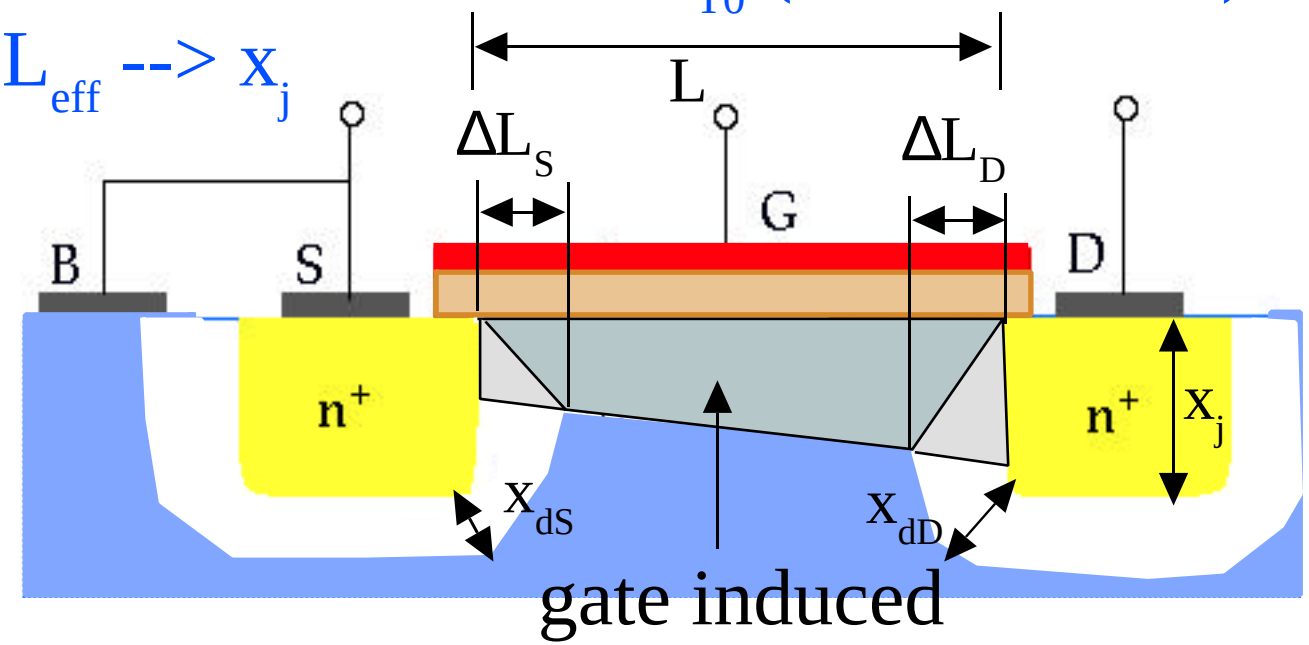
(due to gate voltage across very thin oxide-depletion layer)

$$\mu_n(\text{eff}) = \frac{\mu_{n0}}{1+\Theta E_x} \approx \frac{\mu_{n0}}{1+\eta(V_{GS}-V_T)}$$



Short Channel Effect - V_{T0} (short channel) = V_{T0} - ΔV_{T0}

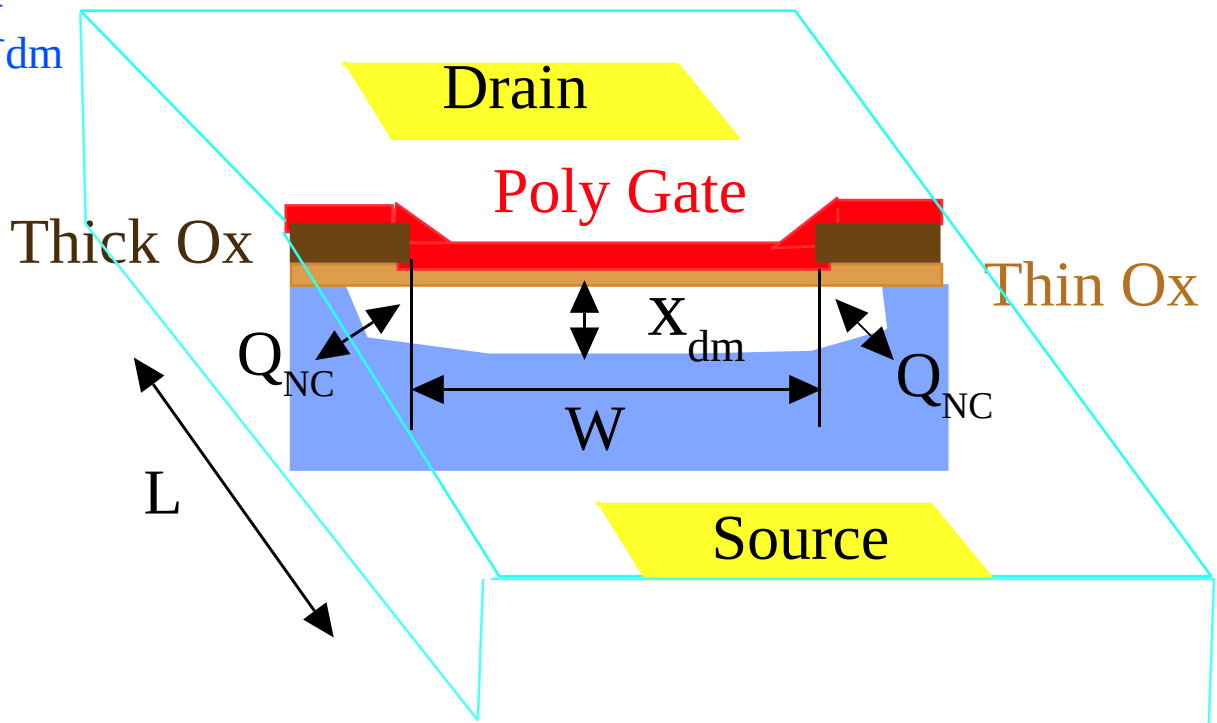
L_{eff} --> x_j



$$\Delta V_{T0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A|2\varphi_F|}\,\frac{x_j}{2L}\left[\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right]+\left[\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right]$$

Narrow Channel Effect - V_{T0} (narrow channel) = V_{T0} + ΔV_{T0}

W --> x_{dm}



$$\Delta V_{T0} = \frac{1}{C_{ox}} \sqrt{2 q \varepsilon_{Si} N_A |2\varphi_F|} \frac{\kappa x_{dm}}{W}$$

SPICE MODELING OF MOS CAPACITANCES

```
M1   4   3   5   0  NFET W=4U  L=1U   AS=15P   AD=15P   PS=11.5U  PD=11.5U
.
.
.
.MODEL NFET NMOS
+ TOX=200E-8
+ CGBO=200P  CGSO=300P  CGDO=300P
+ CJ=200U   CJSW=400P  MJ=0.5  MJSW=0.3  PB=0.7
```

Units: W, L: m; AS, AD: m^2; PS, PD: m; TOX: cm; CGBO, CGSO, CGDO: F/m; CJ: F/m^2; CJSW: F/m; PB: V

U = 10^{-6}

P = 10^{-12}

```
M1   4   3   5   0  NFET W=4U  L=1U   AS=15P   AD=15P   PS=11.5U  PD=11.5U
     D   G   S   B
```

$$C_{gb} = W \times L \times C_{ox} = 4 \times 1 \times 17 \times 10^{-4}\ \text{pF} = 0.0068\ \text{pF}$$

```
M1   4   3   5   0  NFET W=4U  L=1U   AS=15P   AD=15P   PS=11.5U  PD=11.5U
.
.MODEL NFET NMOS
+ TOX=200E-8
+ CGBO=200P  CGSO=300P  CGDO=300P
+ CJ=200U   CJSW=400P  MJ=0.5  MJSW=0.3  PB=0.7
```

$$C_j = \text{Area} \times CJ \times \left(1 - \frac{V_j}{PB}\right)^{-MJ} + \text{Periphery} \times CJSW \times \left(1 - \frac{V_j}{PB}\right)^{-MJSW}$$

CJ = zero-bias junction capacitance per junction area

(200×10^{-6} F/m^2 = 2×10^{-4} pF/μm^2)

CJSW = zero-bias junction capacitance per junction periphery

(400×10^{-12} F/m = 4×10^{-10} pF/μm)

MJ = grading coefficient of junction bottom (0.5)

MJSW = grading coefficient of junction side-wall (0.3)

VJ = the junction potential (V_{sb}, V_{db} for n-channel, V_{bs}, V_{bd} for p-channel)

PB = the built-in voltage (+0.7 V)

Area = AS or AD, the area of source or drain (15×10^{-12} m^2 = 15 μm^2)

Periphery = PS or PD, the periphery of source or drain

(11.5×10^{-6} m = 11.5 μm)