MOS Push-Pull Inverter Amplifier

The push-pull inverter is used extensively in logic circuits due to it's low power dissipation. In the inverting amplifier mode current will flow through due to VDD/2 being applied to each gate.

Note output will be rail-rail.

The circuit of the push-pull inverting amplifier is shown in Figure 1.

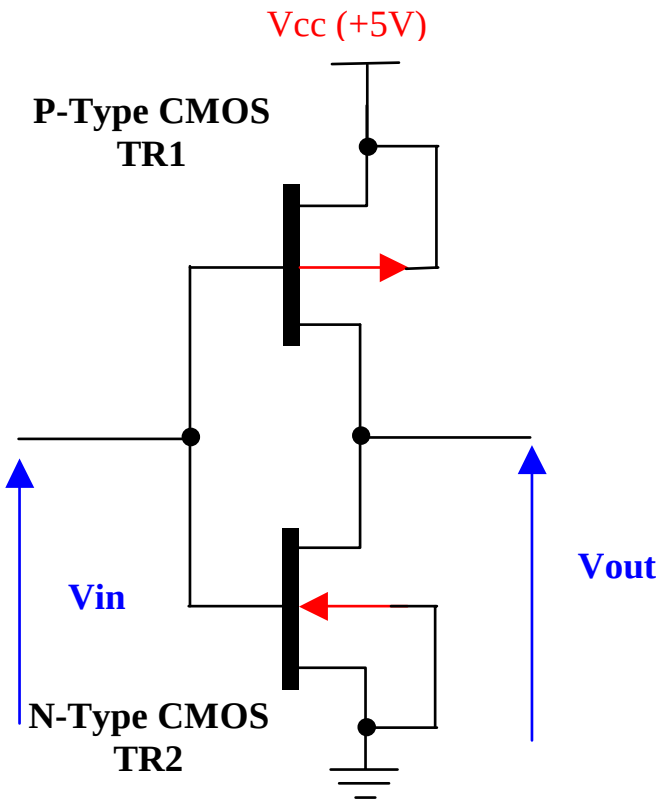

Figure 1 Push-Pull CMOS Inverter circuit.

Note the Bulk/substrate connections (shown by the RED arrow), N-type bulk is connected to t he lowest voltage in this case 0V and the P-type connected to the highest voltage in this case Vcc (+5V).

$$A_V = \sqrt{\frac{2}{I_D}}\left[\frac{\sqrt{K_N \frac{W_1}{L_1}} + \sqrt{K_P \frac{W_2}{L_2}}}{\lambda_1 + \lambda_2}\right]$$

$$R_{OUT} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{I_{DS}(\lambda_1 + \lambda_2)}$$

Example1 Calculate the gain of a push-pull active inverter with W/L ratios of 1 for the N-type device and W/L = 2 for the P-type device, K_N=110uA/V^2, K_P=50uA/V^2, λ = 0.05; V_T = 0.7V. Calculate I_D.

$$\text{Let voltage to each gate} = \frac{V_{DD}}{2} = 2.5V$$

$$I_D = \frac{K_N.W}{2.L}\left(\frac{V_{DD}}{2} - V_T\right)^2 = \frac{110E^{-6}.1E^{-6}}{2.1E^{-6}}\left(\frac{5}{2} - 0.7\right)^2 = 178uA$$

$$A_V = \sqrt{\frac{2}{I_D}}\left[\frac{\sqrt{K_N\frac{W_1}{L_1}} + \sqrt{K_P\frac{W_2}{L_2}}}{\lambda_1 + \lambda_2}\right] = \sqrt{\frac{2}{178E^{-6}}}\left[\frac{\sqrt{110E^{-6}(1)} + \sqrt{50E^{-6}(2)}}{0.05 + 0.05}\right] = 20$$

$$R_{OUT} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{I_{DS}(\lambda_1 + \lambda_2)} = \frac{1}{178E^{-6}(0.05 + 0.05)} = 62K\Omega$$