FAIRCHILD SEMICONDUCTOR™

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Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Fairchild Semiconductor's advanced CMOS helps designers achieve these goals.

FACT™ (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50Ω transmission line drive capability (comparable to Fairchild Semiconductor's FAST® bipolar technology family) to offer a complete family of 1.3-micron SSI, MSI, and LSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD, and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to system-generated problems.
- Board Layout—Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling—Maximize ground and V_{DD} traces to keep V_{DD}/ground impedance as low as possible; full ground/V_{DD} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.
- Electromagnetic Interference

Interfacing

FACT and FACT QS devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current under worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive FAST, ALS, AS, LS, HC and HCT devices.

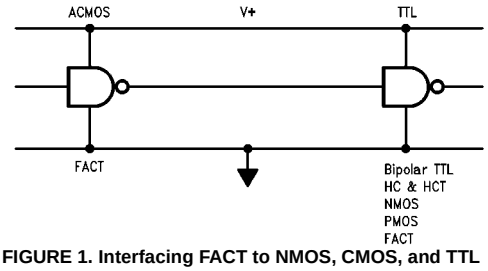

FIGURE 1. Interfacing FACT to NMOS, CMOS, and TTL

FACT devices can be directly driven by both NMOS and CMOS families, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μA per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT AC/ACQ circuits directly; this is due to inadequate output HIGH level capability, which is guaranteed to 2.4V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to V_{DD} of approximately 4.7 kΩ, which is depicted in Figure 2. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.

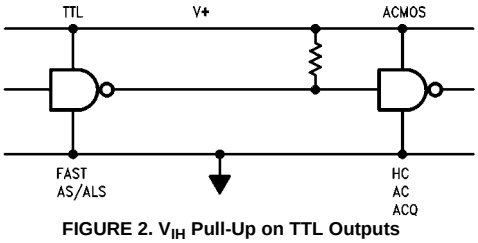

FIGURE 2. V_{IH} Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, Fairchild Semiconductor has designed devices which offer thresholds that are TTL-compatible (Figure 3).

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FACT™ is a trademark of Fairchild Semiconductor Corporation.
VMEbus™ is a trademark of Motorola Incorporated.
MULTIBUS® is a registered trademark of Intel Corporation.

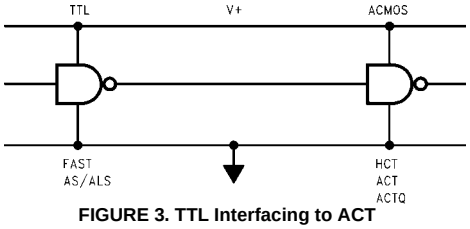


FIGURE 3. TTL Interfacing to ACT

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using a F100324 TTL-to-ECL translator and a F100325 ECL-to-TTL translator in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to V_{DD} of approximately 4.7 kΩ).

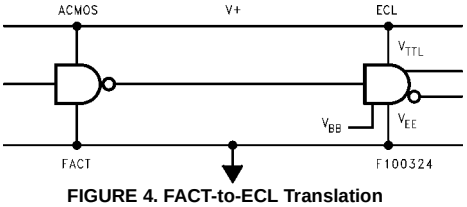


FIGURE 4. FACT-to-ECL Translation

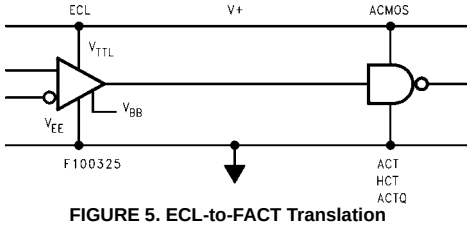


FIGURE 5. ECL-to-FACT Translation

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

Line Driving and Termination

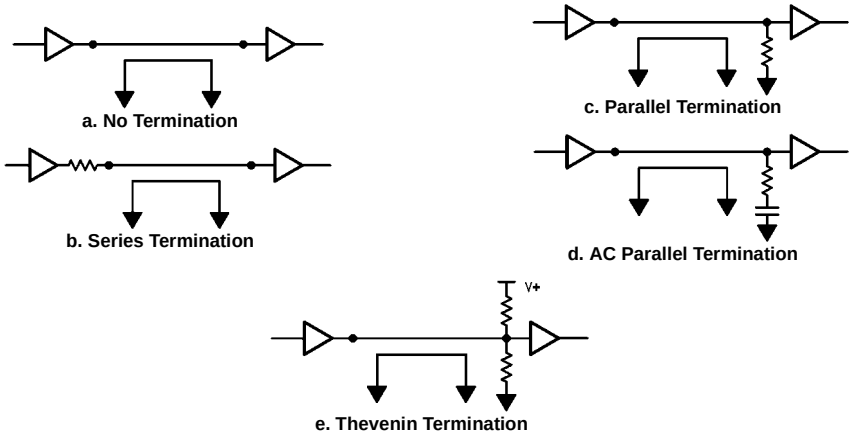


FIGURE 6. Termination Schemes

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft. for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z'_o, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z'_o and t_{pde} can be calculated with:

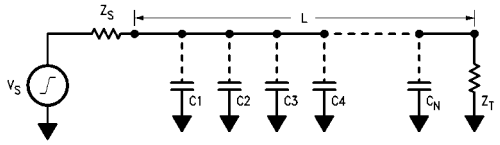
$$Z'_o = \frac{Z_o}{\sqrt{1 + C_D/C_L}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_D/C_L}$$

where C_L = intrinsic line capacitance and C_D = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most

heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.



Length of Transmission Line = L

Distributed Load Capacitance per Unit Length = $C_D = \sum_{n=1}^{N} C_L/L$

Characteristic Impedance of a Transmission Line Altered by Distributed Loading

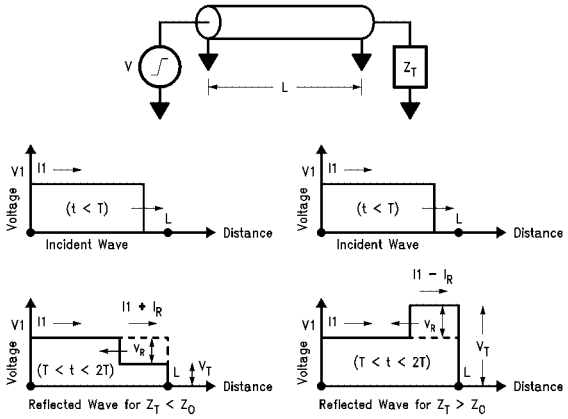
$$= Z'_O$$

$$= \sqrt{\frac{L_O}{C_O + C_D}}$$

$$= \frac{Z_O}{\sqrt{1 + \frac{C_D}{C_O}}}$$

Effective Reflection Coefficient at Termination = $\rho = \frac{Z_T - Z'_O}{Z_T + Z'_O}$

FIGURE 7. Transmission Line with Distributed Loading



- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t
- Incident Wave Current = I_1
- Incident Wave Voltage = V_1
- Reflected Wave Current = I_R
- Reflected Wave Voltage = V_R
- Characteristic Impedance of Line = Z_O
- Termination Impedance = Z_T
- Voltage at Termination = V_T

FIGURE 8. Reflections Due to Impedance Mismatching

There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

NO TERMINATION

No termination is the lowest cost option and features the easiest design. For line lengths 8 inches or less, this is often the best choice. For lines longer than 8 inches, transmission line effects (line delays and ringing) may exist. Figure 9 illustrates the effect of a FACT device driving a 3-foot open-ended coaxial line. Clamp diodes at the inputs of most logic devices tend to reduce the ringing and overshoots. Often these clamp diodes are sufficient to insure reliable system operation. Figure 10 illustrates the impact of these diodes on the same 3-foot coaxial line. However. it is not uncommon to find logic devices like DRAMs, D-to-A converters and PLDs, that have no input clamp diodes.

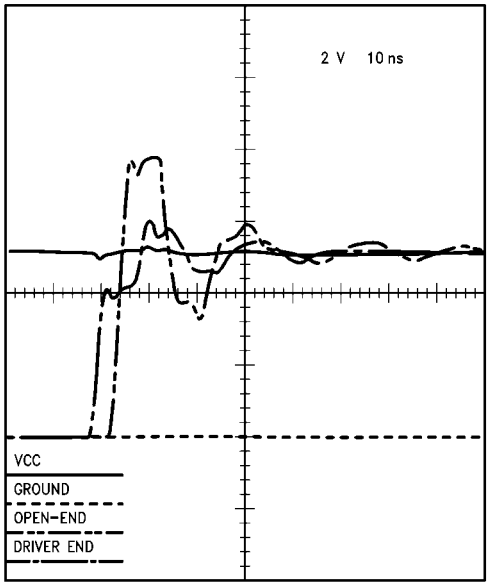


FIGURE 9. Transmission Line Effects
FACT Driving 3 Foot Open-Ended Coax

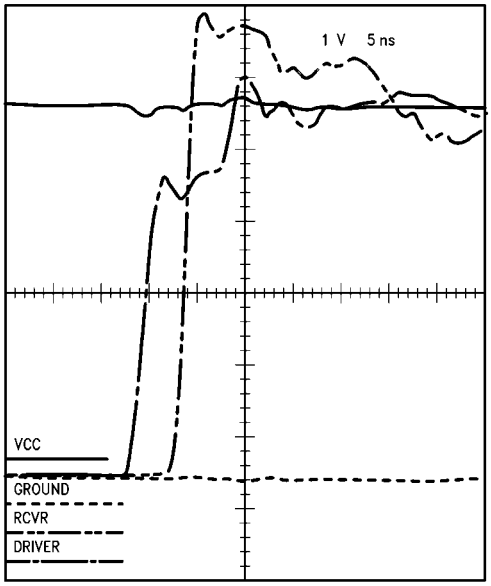


FIGURE 10. Effects of Input Clamp Diodes
FACT Driving FACT with no Termination

SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave, V_i. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of the line according to the formula

$V_i = V_{DD} \bullet Z'_o/(Z'_o + R_S + Z_S)$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. Z_S for FACT is approximately 17Ω. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

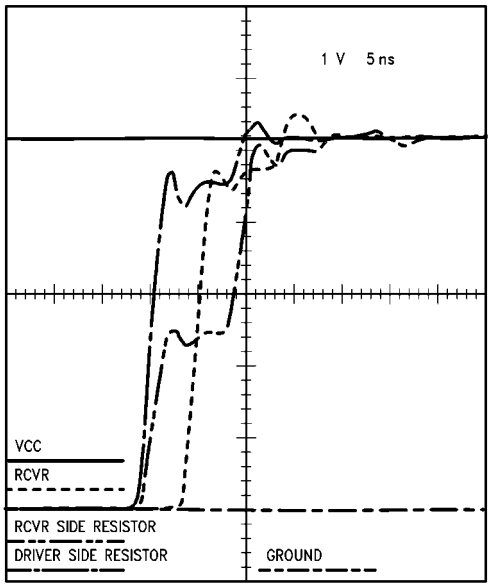


FIGURE 11. FACT Driving FACT
with Series Termination

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{DD} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

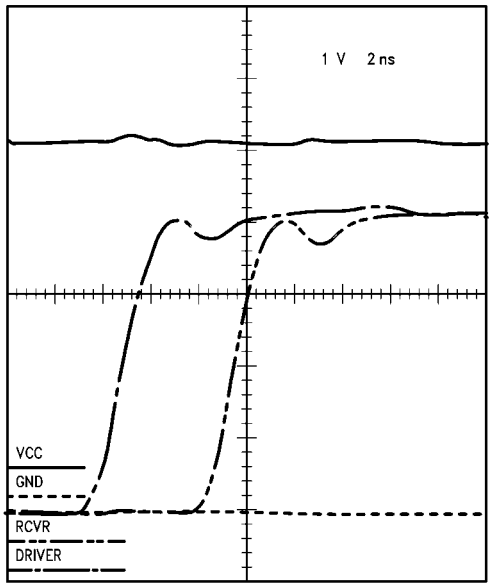


FIGURE 12. FACT Driving FACT with Parallel Termination

AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

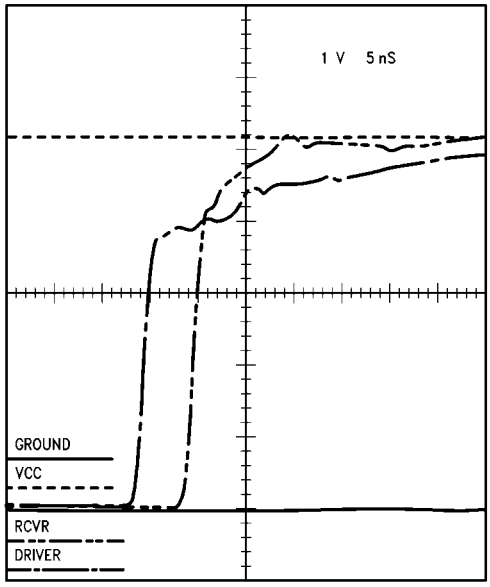


FIGURE 13. FACT Driving FACT with AC Termination

THEVENIN TERMINATION

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle.Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{DD} or ground, increasing power consumption.

- Parallel: Resistor $= Z_o$
- Thevenin: Resistor $= 2 \times Z_o$
- Series: Resistor $= Z_o - Z_{out}$
- AC: Resistor $= Z_o$

  Capacitor $= C \geq \frac{3tr}{Z_o}$

FIGURE 14. Suggested Termination Values

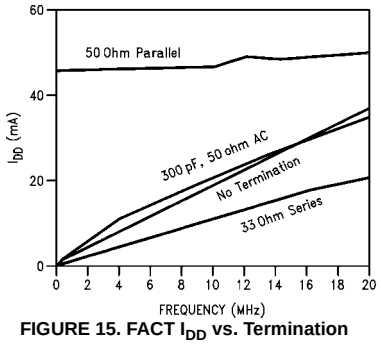


FIGURE 15. FACT I_{DD} vs. Termination

FACT circuits have been designed to drive 50Ω transmission lines over the full commercial temperature range and 75Ω transmission lines over the military temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 75 mA source and sink current. This ensures incident wave switching on 50Ω transmission lines and is consistent with the 3 ns rated edge transition time.

FACT and FACT QS devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} for AC/ACQ devices are specified at 70% and 30% of V_{DD} respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50 μA or less. These noise margins are outlined in Figure 16.

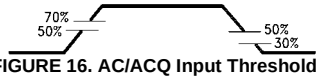


FIGURE 16. AC/ACQ Input Threshold

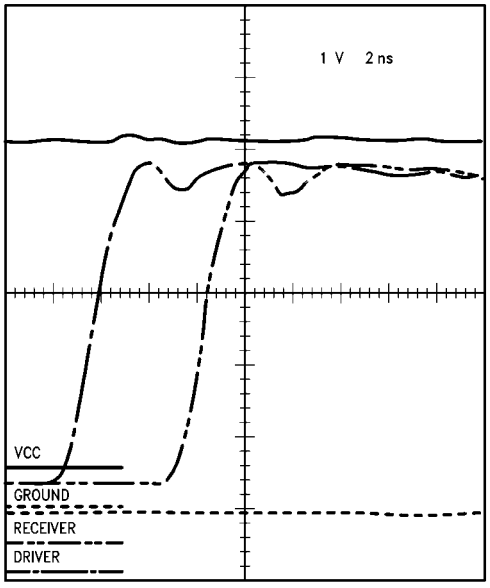


FIGURE 17. FACT Driving FACT with Thevenin Termination

CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{DD} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 18 exemplifies the situation when power is removed. Any input driven above the V_{DD}pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{DD} or any output that is HIGH. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line. Another possible solution would be to ensure that the output enable input is inactive, preventing the outputs from turning on and loading down the bus. This may be accomplished by hardwiring a 4.7 kΩ pull-up resistor to the V_{DD}pin of the FACT device.

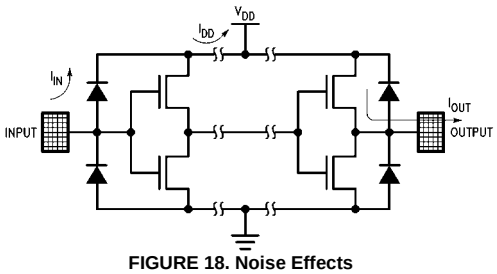


FIGURE 18. Noise Effects

Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{DD} and outputs that drive to within 100 mV of the rails, FACT AC/ACQ devices offer noise margins approaching 30% of V_{DD}. At 5V V_{DD}, FACT's specified input and output levels give almost 1.5V of noise margin for both ground- and V_{DD}-born noise. With realistic input thresholds closer to 50% of V_{DD}, the actual margins approach 2.5V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

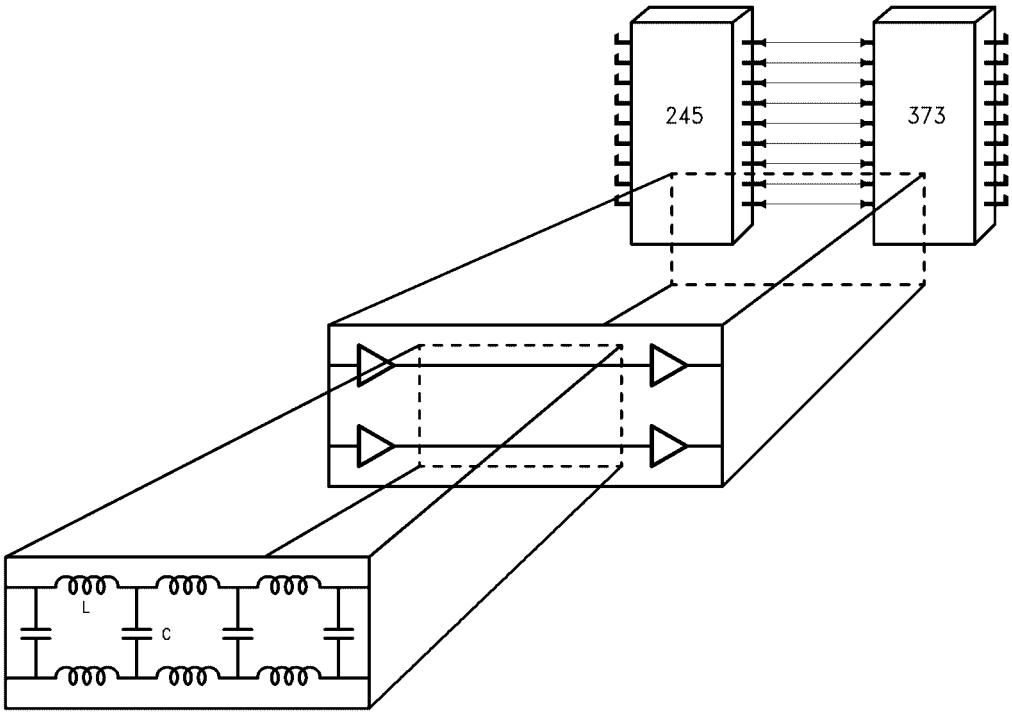
Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, Figure 20 and Figure 22, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (ϵ_r = 1.0) and epoxy glass (ϵ_r = 4.7). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

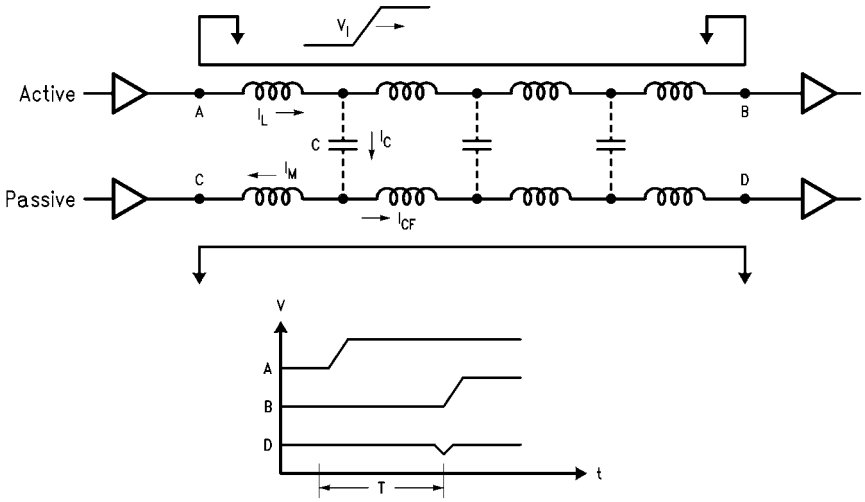
Reverse crosstalk, Figure 21 and Figure 23, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in Figures 25, 27, 28, 26, 29, 30, exemplify the outstanding immunity to everyday noise which can effect system reliability.



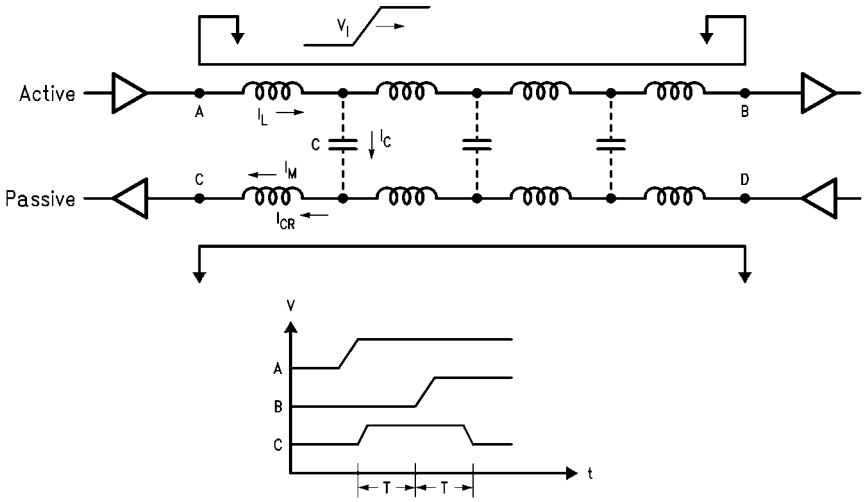
- Two parallel signal lines provide mutual inductance and shunt capacitance

FIGURE 19. Where Does Crosstalk Take Place?



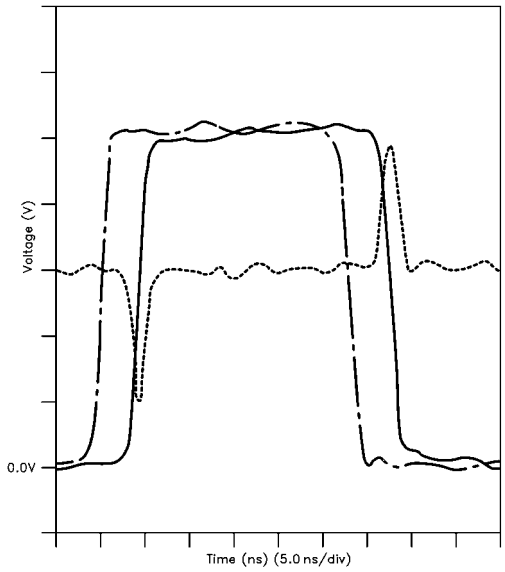
- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = $I_C = -C\ dV_I/dt$
- Mutually Induced Current = $I_M = mI_L$
- Forward Crosstalk Current = I_{CF}
- As the active signal, V_I, propagates from A to B a negative-going spike, V_f, propagates from C to D, coincident with V_I.

FIGURE 20. Forward Crosstalk—Refresher



- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = $I_C = -C\ dV_I/dt$
- Mutually Induced Current = $I_M = mI_L$
- Reverse Crosstalk Current = I_{CR}
- As the active signal, V_I, propagates from A to B a positive pulse appears at C for a duration twice the coupled line delay T.

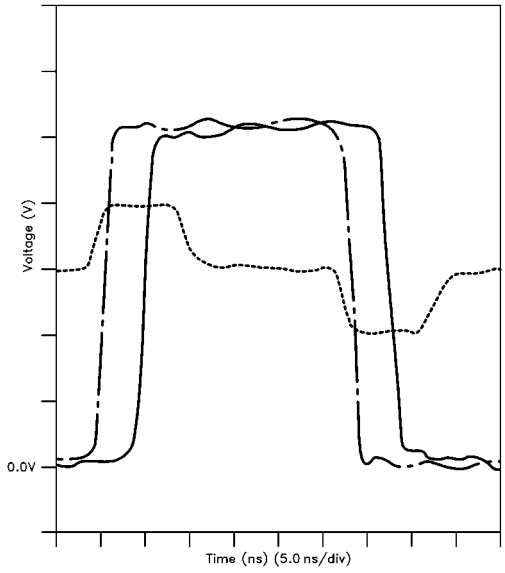
FIGURE 21. Reverse Crosstalk—Refresher



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

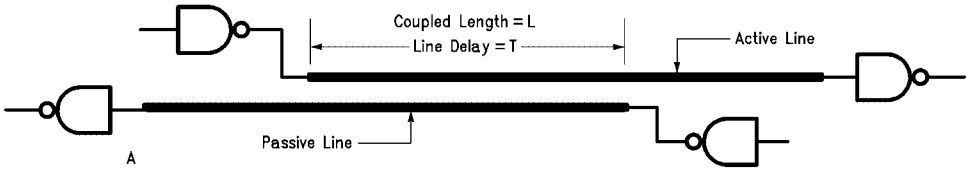
FIGURE 22. Forward Crosstalk on PCB Traces



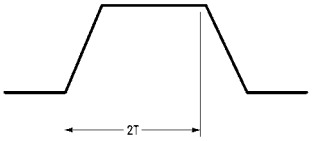
Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

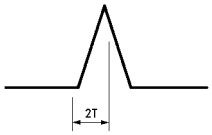
FIGURE 23. Reverse Crosstalk on PCB Traces



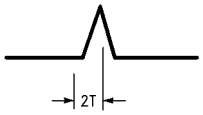
Noise Pulses at A:



For $T > t_r$ Noise Reaches Max Amplitude



For $T = 0.5\ t_r$ Noise Just Reaches Max at Peak



For $T < 0.5\ t_r$ Noise Never Reaches Full Amplitude

FIGURE 24. Partially Coupled Lines

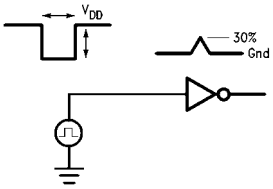


FIGURE 25. High Noise Margin

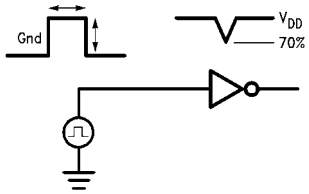


FIGURE 26. Low Noise Margin

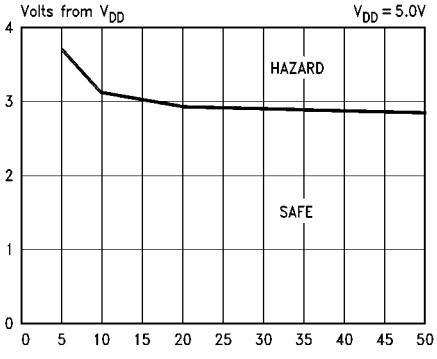


FIGURE 27. FACT AC/ACQ High Noise Margin

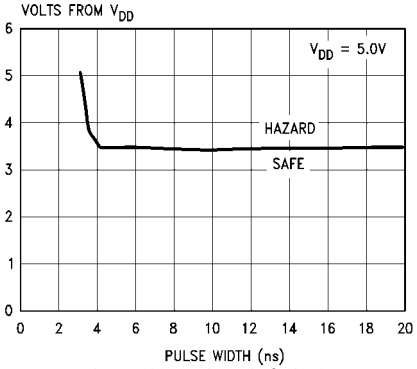


FIGURE 28. FACT ACT/ACTQ High Noise Margin

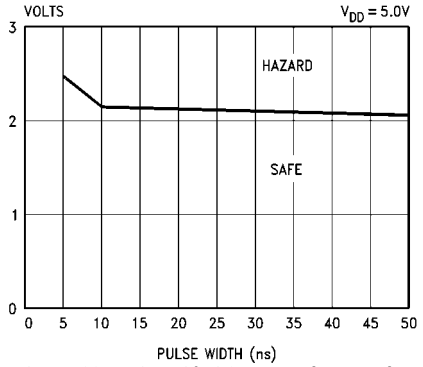


FIGURE 29. FACT AC/ACQ Low Noise Margin

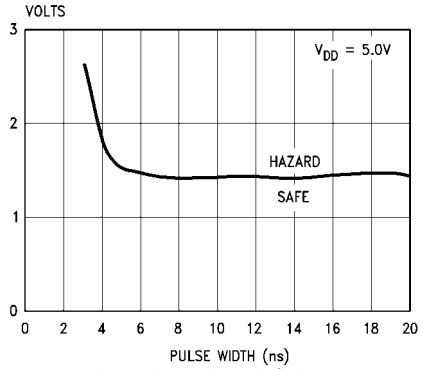


FIGURE 30. FACT ACT/ACTQ Low Noise Margin

With over 2.0V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

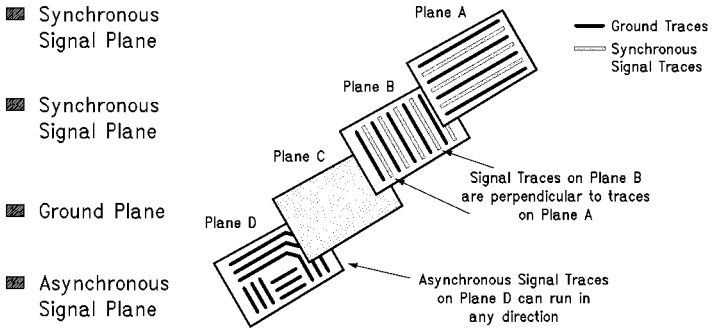


FIGURE 31. Recommended Crosstalk—Avoidance Structure

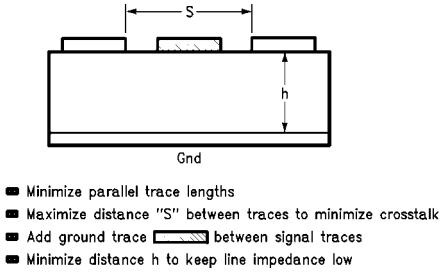


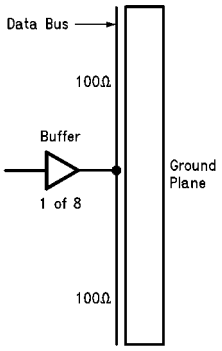
FIGURE 32. PCB Layout Tips for Crosstalk Avoidance

Decoupling Requirement

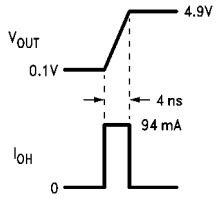
Fairchild Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 34 displays various $V_{DD}$and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50Ω and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{DD} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 34 to calculate the amount of decoupling necessary. This circuit utilizes an AC240 driving a 100Ω bus from a point somewhere in the middle.



Buffer Output Sees Net 50Ω Load. 50Ω Load Line on I_{OH}–V_{OH} Characteristic. Shows LOW-to-HIGH Step of Approximately 4.8V.



Worst-Case Octal Drain = 8 × 94 mA = 0.75 Amp.

FIGURE 33. Octal Buffer Driving a 100Ω Bus

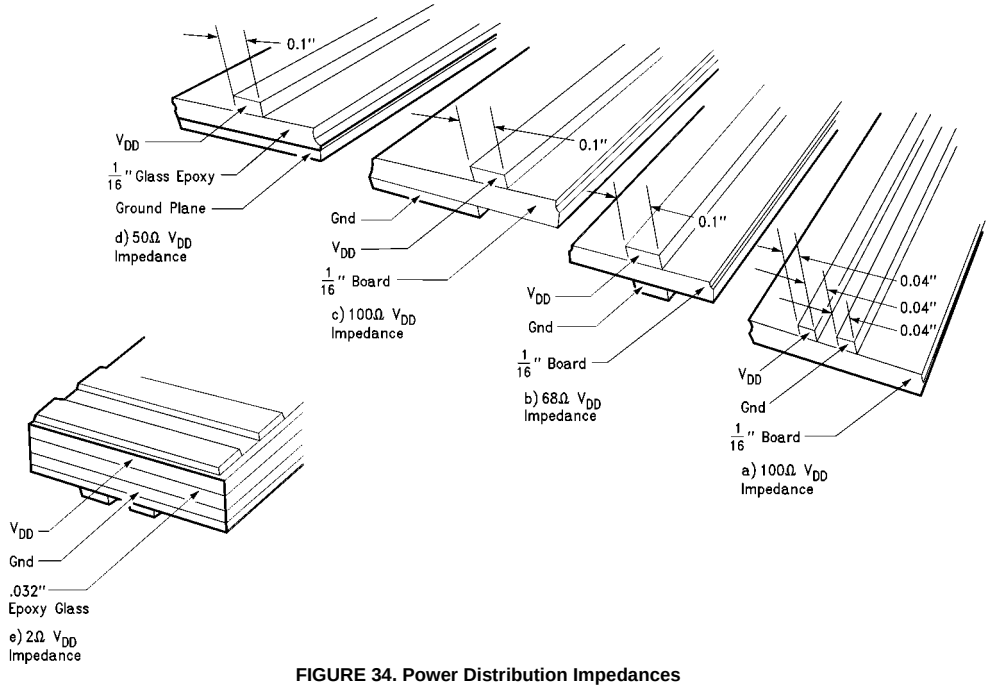


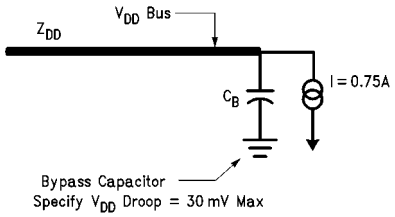
FIGURE 34. Power Distribution Impedances

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{DD} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the volt-

age within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 35.

In this example, if the V_{DD} droop is to be kept below 30 mV and the edge rate equals 4 ns, a 0.10 µF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



$Q = CV$

$I = C\Delta V/\Delta t$

$C = I\Delta t/\Delta V$

$t = 4 \times 10^{-9}$

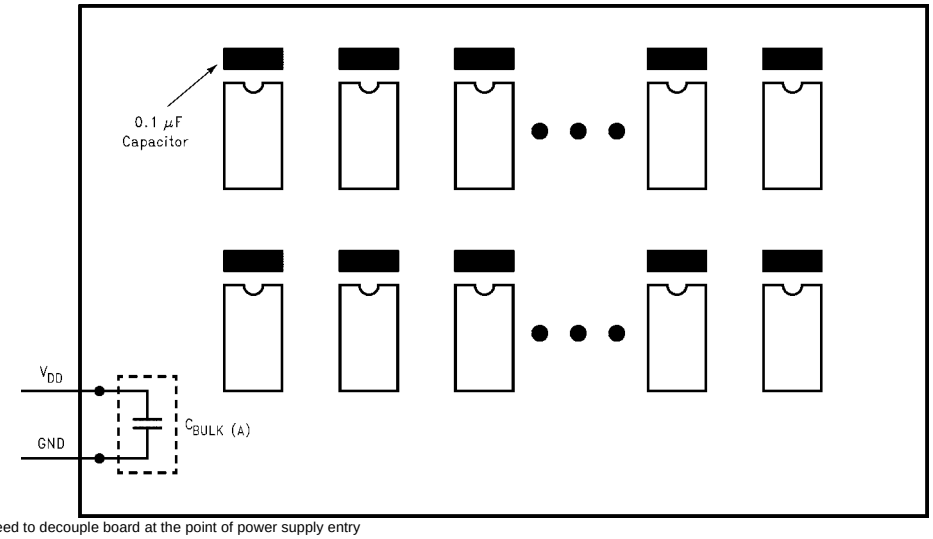
$$C = \frac{0.750 \times 4 \times 10^{-9}}{0.03} = 100 \times 10^{-9} = 0.100\ \mu F$$

Select $C_B \geq 0.10\ \mu F$

FIGURE 35. Formula for Calculating Decoupling Capacitors

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 µF–100 µF)

FIGURE 36. Board-Level Decoupling Capacitor

Electromagnetic Interference

One of the features of advanced CMOS is its fast output edge rates. For the first time a non-ECL logic family is capable of switching outputs at ECL speeds. In fact, advanced CMOS edge rates exceed that of ECL. ECL outputs typically swing 900 mV in 700 ps, translating into an edge rate of 1.3 V/ns. Advanced CMOS outputs, on the other hand, swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted.

EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibility.

SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

As Figure 37 illustrates, EMI in a typical electronic circuit is generated by a current flowing in some current path configured within the circuit. These paths can be either V_{DD}-to-GND loops or output transmission lines. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The current path material itself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. Figure 38 illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the frequency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

OVERALL SYSTEM EMI

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—V_{DD}-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components.

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \bullet I \bullet A \bullet Freq^2}{D} \left[1 + \left(\frac{\lambda}{2} \pi D \right)^2 \right]^{1/2} \frac{\mu V}{m}$$

where,

$|E|_{Max}$ is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the antenna area in square cm

λ is the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop $P \ll \lambda$.

Figures 39, 40 illustrate lab measurements of radiated emissions from a test board populated with FACT, FACT QS, and a competitor's ACMOS logic. The device under test is driving a similar device across 26 cm of printed circuit board trace.

At higher frequencies where, for example, quarter wavelengths approach the lengths of transmission lines common in typical backplanes and plug-in cards, FACT QS with its innovative noise suppressions circuitry radiates substantially less EMI than other ACMOS logic.

CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data transmission or unreliable system operation. Therefore, good EMC design techniques at the circuit board level are just as necessary.

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several

orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.

- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplines or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 8 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undesirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

- On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.
- Decoupling the power supply at the point of entry onto the printed circuit board is also highly recommended. The use of a low equivalent series inductance, or ESL, multilayer ceramic capacitor, 50 μF to 100 μF, provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10 μF chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

BACKPLANE CONSIDERATIONS

The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used.

- Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC.
- Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors.

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.

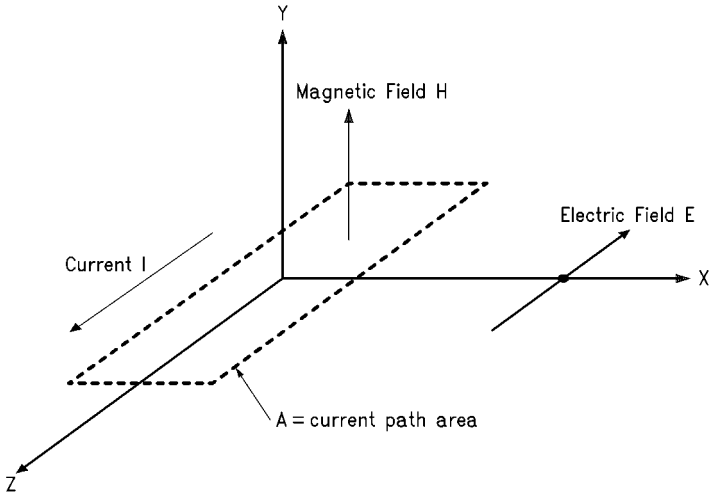
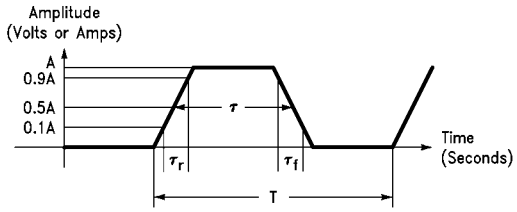


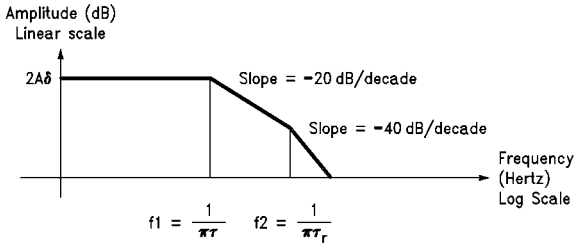
FIGURE 37. EMI is Generated by a Current Flowing along Some Path (Loop)

Time Domain: Trapezoidal Pulse Train



- τ = Pulse Width HIGH
- τ_r = Rise Time
- τ_f = Fall Time
- T = Period
- A = Amplitude

Frequency Domain: Worst-Case Upper Bound Approximation



- f_1 = 1st Breakpoint
- f_2 = 2nd Breakpoint
- δ = Duty Cycle = τ/T

FIGURE 38. Time Domain to Frequency Domain Conversion

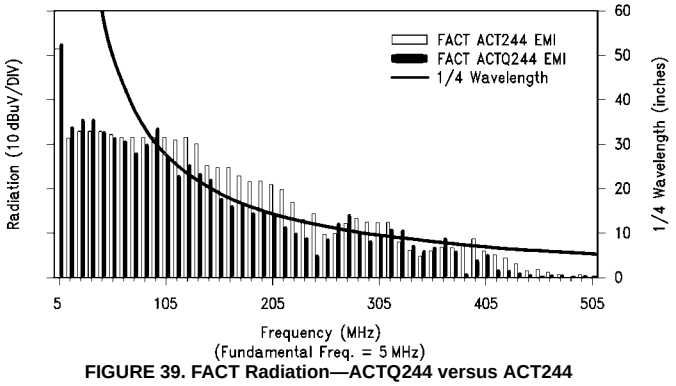


FIGURE 39. FACT Radiation—ACTQ244 versus ACT244

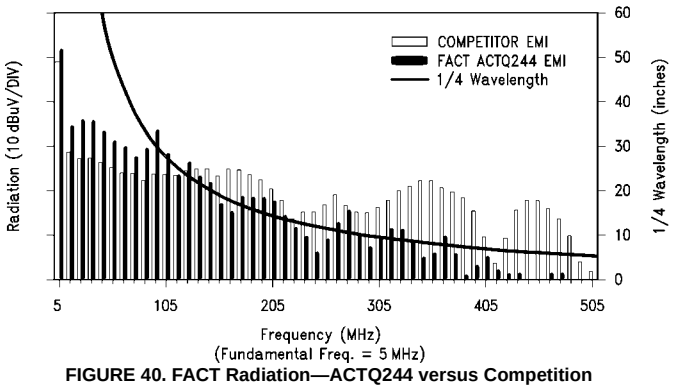


FIGURE 40. FACT Radiation—ACTQ244 versus Competition

TTL-Compatible CMOS Designs Require Delta I_{DD} Consideration

The FACT product line is comprised of two types of advanced CMOS input circuits: AC/ACQ and ACT/ACTQ devices. ACT/ACTQ indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As these ACT/ACTQ series are used to replace TTL, the I_{DDT} or Delta I_{DD}specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS. In many datasheets I_{DDT} or Delta I_{DD} are also referred to as I_{CCT} or Delta I_{CC}. There are no other differences.

It is important to understand the concept of Delta I_{DD} and how to use it within a design. First, consider where Delta I_{DD} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.

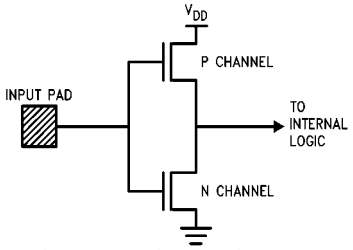


FIGURE 41. FACT Input Structure

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 4 kΩ while the resistance of an OFF transistor is generally greater than 500 MΩ. When the input to this structure is at either ground or V_{DD}, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 500 MΩ. The leakage current will then be less than 1 µA. When the input is between ground and V_{DD}, the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600Ω. This reduction in series resistance of the input structure will cause a corresponding increase in I_{DD}as current flows through the input structure. The following graph depicts typical I_{DD} variance with input voltage for an ACT device.

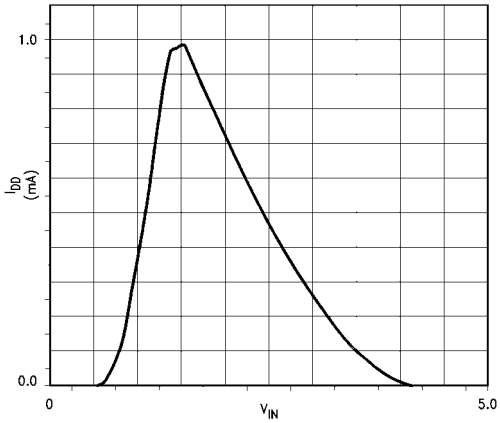


FIGURE 42. I_{DD} versus Input Voltage for ACT Devices

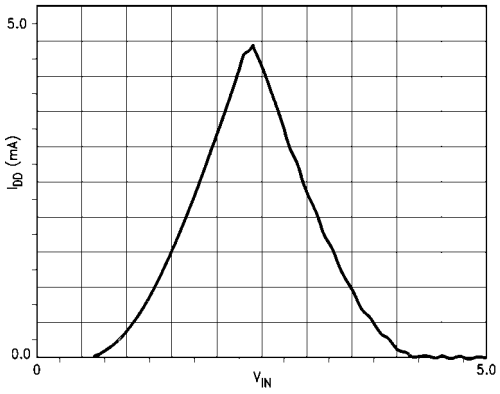


FIGURE 43. I_{DD} versus I_{IN} for AC Devices

The Delta I_{DD} specification is the increase in I_{DD}. For each input at V_{DD} − 2.1V (approx. TTL V_{OH} level), the Delta I_{DD} value should be added to the quiescent supply current to arrive at the circuit's worst-case static I_{DD} value.

Fortunately, there are several factors which tend to reduce the increase in I_{DD} per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive ACT-type inputs down to 200 mV and up to 3.5V. Additionally, the typical I_{DD} increase per input will be less than the specified limit. As shown in the graph above, the I_{DD} increase at V_{DD} − 2.1V is less than 200 μA in the typical system. Experiments have shown that the I_{DD} of an ACT240 series device typically increases only 200 μA when all of the inputs are connected to a FAST device instead of ground or V_{DD}.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{DD} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the 245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for $I_{DD}$and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{DD} specification orders of magnitude less than standard load currents. Most CMOS I_{DD} specifications are usually less than 100 μA. When conducting an I_{DD} test, greater care must be taken so that other currents will not mask the actual I_{DD} of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{DD} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{DD} test. Even a standard 500Ω load resistor will sink 10 mA at 5V, which is more than twice the I_{DD} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{DD} tests.

Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{DD} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from V_{DD} to ground. This conduction path leads to the increased I_{DD} current seen in the I_{DD} vs. V_{IN} curve. When the input is at either rail, the input structure no longer conducts. Most I_{DD} testing is done with all of the inputs tied to either V_{DD} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{DD} of the device under test which is being measured by the tester.

When testing the I_{DD} of a CMOS 245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.

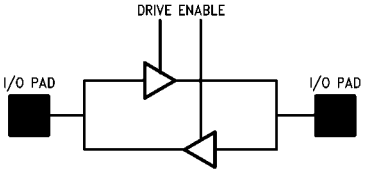


FIGURE 44. 245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{DD} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and

allowed to float, the input device will also float, and an excessive amount of current will flow from $V_{DD}$to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an I_{DD} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. This combined leakage test is defined as IOZ_T. For FACT devices, I_{IN} is specified at ±1 µA while I_{OZ} is specified at ±5 µA. Combining these gives a limit of ±6 µA for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.

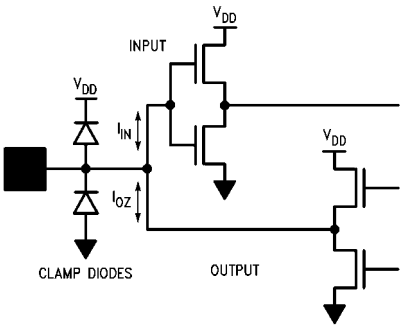


FIGURE 45. FACT I/O Pin Internal Structure

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of 3-STATE Outputs in a Transmission Line Environment

Traditionally, the disable time of a 3-STATE buffer has been measured from the 50% point on the disable input, to the (V_{OL} + 0.3V) or (V_{OH} − 0.3V) point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

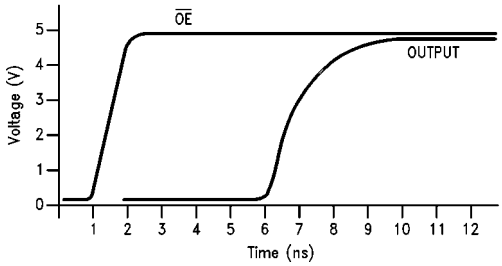


FIGURE 46. Typical Bench 3-STATE Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

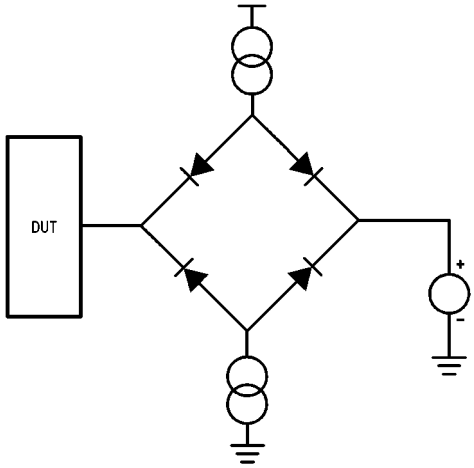


FIGURE 47. MCT Wheatstone Bridge Test Load

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the (V_{OL} + 0.3V) level or fallen to the (V_{OH} − 0.3V) level.

Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in Figure 48.

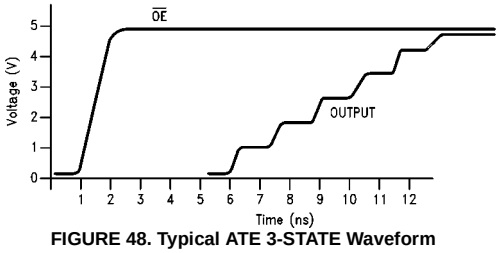


FIGURE 48. Typical ATE 3-STATE Waveform

Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50Ω to 60Ω, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the disable measurement points, it would be looking for a step of approximately 575 mV at 5.5V V_{DD}. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customer's incoming tests, even though the device meets specifications. Figure 49 graphically shows this stepout.

Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.

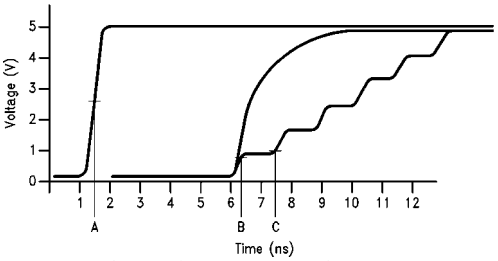


FIGURE 49. Measurement Stepout