High-speed Sigma-Delta Analog-to-Digital Conversion for Indoor Wireless Systems

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Introduction

- **System Specifications for ADC**
  - 25 Ms/s Nyquist rate. (T_{chip} = 40ns)
  - Approx. 6-8+ bits dynamic range.

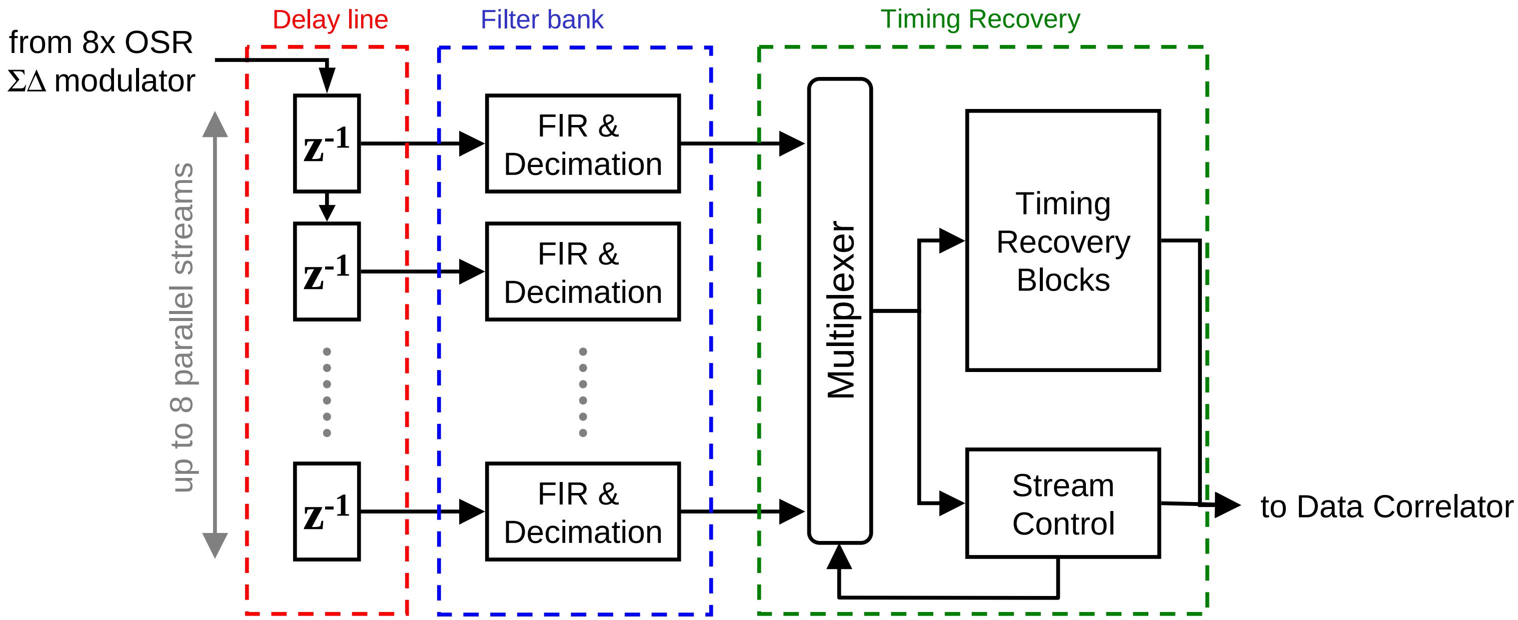
    see C. Teuscher, “Low Power Receiver Design for Portable RF Applications…,” Ph.D. thesis, UCB ’98
  - Sampling offset granularity < $T_{chip}/2$.
- **Choice of converter architecture**
  - Specification met with pipeline converter

    see G. Chien, “High-Speed, Low-power, Low-Voltage, Pipelined A/D Converter,” MS thesis, UCB ’96.
  - High f_T of 0.25µm CMOS makes sigma-delta (ΣΔ) architecture feasible.

Motivation for ΣΔ Converter

- **Leverage off of increasing f_T of CMOS process.**
  - f_{NYQ} of high-resolution ΣΔ's > 2 MHz.
- **Decreased sensitivity to analog mismatch and other imperfections**
  - Calibration or digital correction not necessary.
- **Oversampling eases requirements of supporting analog filtering.**
- **Oversampling decreases area used by passives.**
- **ΣΔ is a "mostly digital" converter**
  - Robust, programmable digital channel-select filters
  - Opportunities for system/circuit co-design.

ΣΔ-assisted Timing Recovery

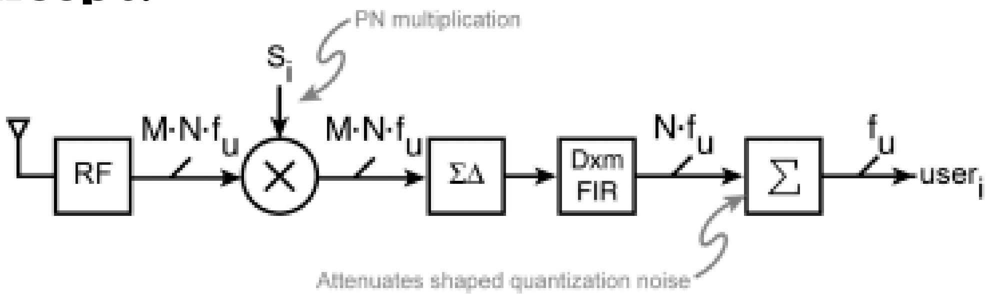


$T_{chip}/8$ sampling offset granularity with A/D running at Nyquist

Architectural modifications can reduce filter bank complexity with an increase in stream-switching latency

Code-based Noise Shaping

- **Equivalence of FDMA and CDMA systems**
  - Both systems divide bandwidth into *N* subsets.
  - Only difference is basis of *N*-dimensional space.
- **ΣΔ modulators "shape" noise out of desired subset**
  - FDMA systems shape q-noise into other frequency band.
  - Can we extend this to CDMA?
- **First concept:**



  - Analog PN-sequence.
  - Achieves effective oversampling of *M*N*.

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High-Speed ΣΔ Architecture Considerations

- **High-speed ΣΔ: low-oversampling (OSR).**
- **Low-OSR: high order, multi-bit ΣΔ.**
- **High-order ΣΔ: Single-loop vs. cascade**

  Single-loop high-order modulators can be unstable

  Cascade ΣΔ's more sensitive to analog non-idealities; interstage coupling amplifies noise.
- **Single-bit vs. multibit quantization**

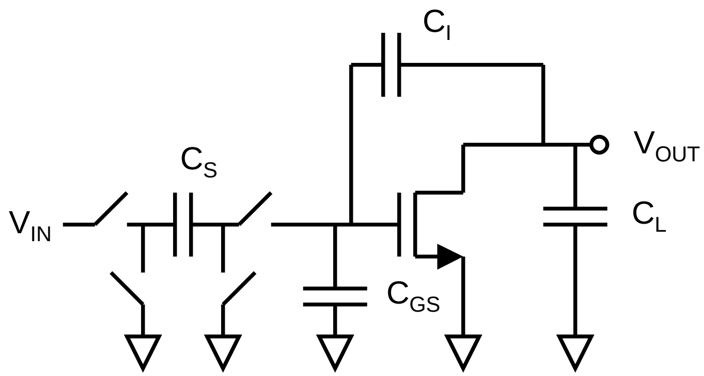
  Multi-bit converter reduces quantization noise

  Multi-bit DAC in first stage must be highly linear.

  Non-linearity of multi-bit DAC in later stages is shaped.

ΣΔ Architecture and Static Power Dissipation

- **Typical SC integrator:**



$$I \propto g_M$$

$$V_{SW} = \beta \cdot V_{DD}$$

$$DR = \frac{P_{SIG}}{P_{NOISE}} \propto \frac{\left(\frac{V_{SW}^2}{8}\right)}{\left(\frac{kT}{M \cdot C_S}\right)}$$

$$C_S = A \cdot C_I$$

$$C_{GS} = g_M / \omega_T$$

$$C_L = \eta \cdot C_S$$

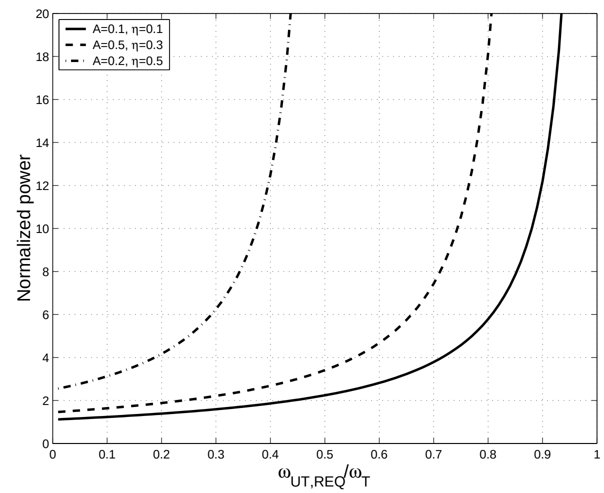
$$\omega_{U,REQ} = \chi \cdot M \cdot f_N$$

- **P_{STAT} without parasitics:**

$$P_{STAT} \propto \frac{8kT(DR)\chi \cdot f_N}{\beta^2 V_{DD}}$$

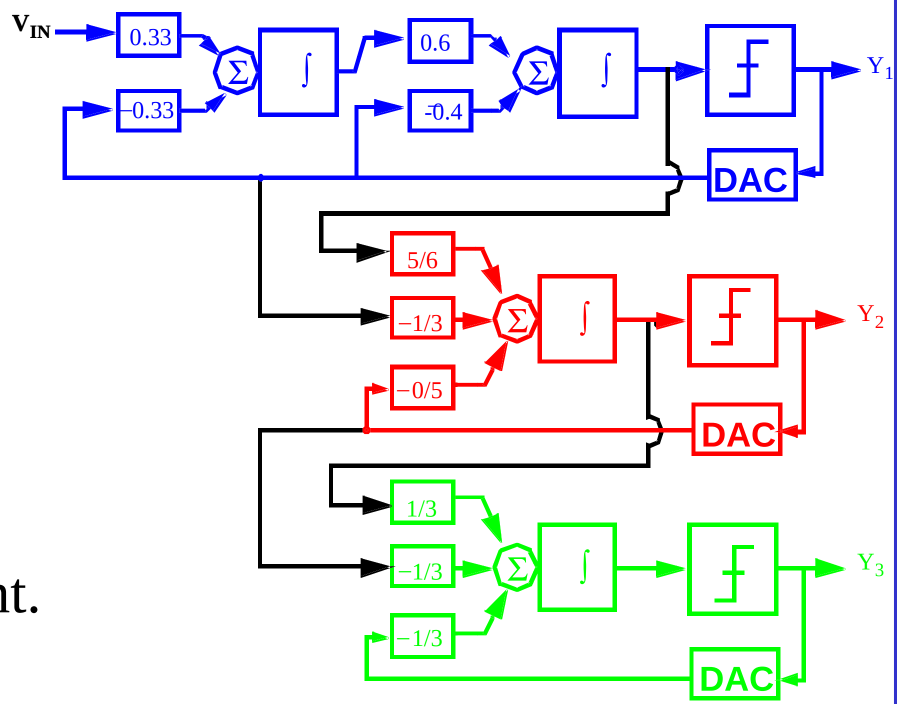
- **P_{STAT} with parasitics:**

$$P_{STAT} \propto \frac{8kT(DR)\chi \cdot f_N}{\beta^2 V_{DD}} \cdot \frac{(1+\eta+A\eta)}{\left(1-\frac{\omega_{U,REQ}(1+A\eta)}{\omega_T}\right)}$$

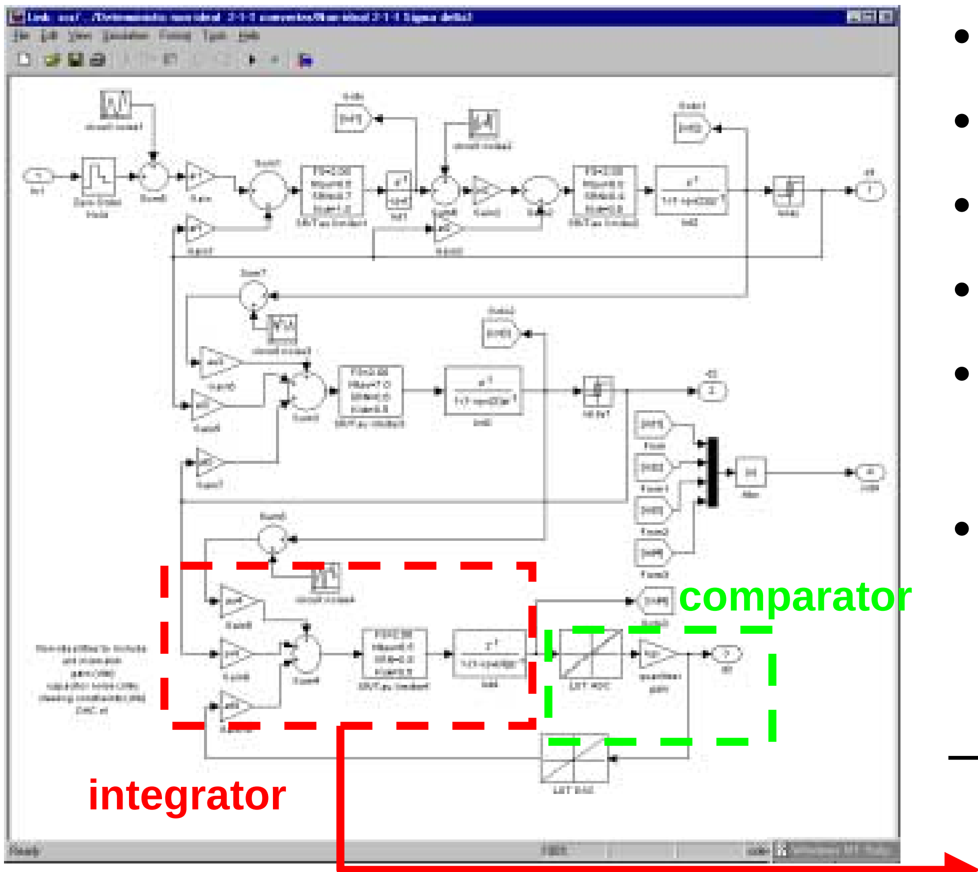


2-1-1 Cascade Architecture

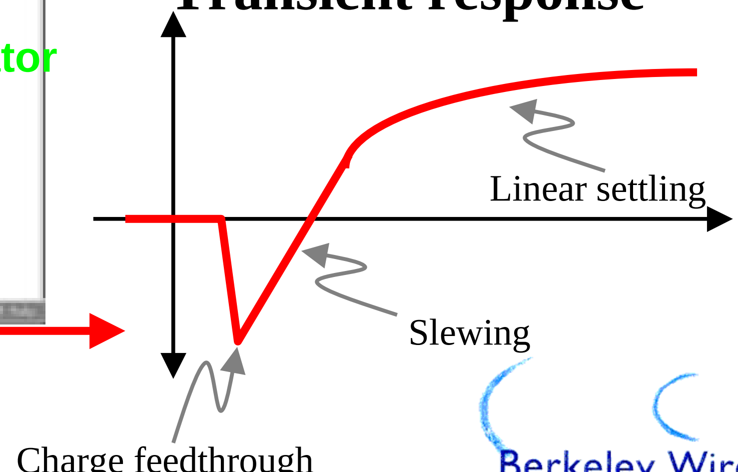
- **Architecture Choice:**
  - 2-1-1 cascade. OSR=8.
  - 1-bit quantization in all stages
  - DR = 47 dB
- **Coefficient Selection**
  - Small coefficients alleviate speed constraints.
  - Thermal noise not dominant.



Structural System Modeling, ΣΔ Modulator



- Quantization noise
- Thermal noise
- Finite DC gain
- Capacitor mismatch
- Comparator offset, hysteresis
- Transient response



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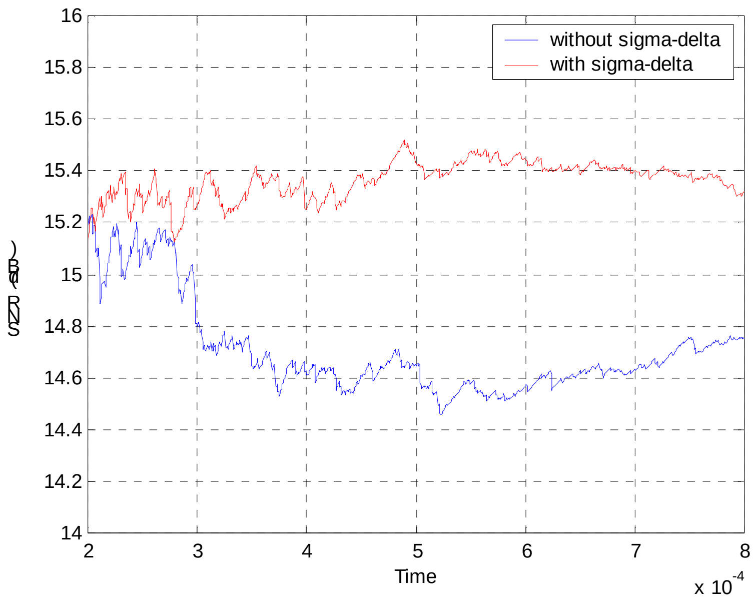
ΣΔ and Downlink block-level simulation

- **Circuit blocks modelled in SIMULINK.**
- **ΣΔ simulated as part of entire downlink.**

Circuit reqt's for 47 dB DR

DC Gain	A_{vo}	>80
Capacitor mismatch	$\sigma_{\Delta C/C}$	< 5%
Comparator offset	v_{os}	< 120 mV
3dB frequency	f_{3dB}	> 550 MHz
Phase margin	ϕ_m	> 60 deg
Differential Slew Rate	SRN	> 900 V/μs

SNR of complete downlink (SIMULINK model)



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Circuit Design

- **Integrators**
  - Speed requirement dominant; low gain requirement.
  - NMOS folded cascode topology:
    - $A_{v0} = (g_m r_o)^2$ is sufficient.
    - NMOS input for maximum speed.
    - Folded cascode for swing. Sufficiently stable.
  - Developed optimization routine to minimize power.
- **Switches**
  - V_{GS} limited to 2.5V. Process not tolerant of standard bootstrap.
  - “Constant V_{GS} bootstrap” loads signal path.
  - CMOS switches utilized. Increased clock power.
- **Comparator**
  - High input offset, hysteresis tolerable.
  - Low-power dynamic comparator used

Simulation Results

- **Simulated DR: 47 dB**
  - Q-noise limited
- **25 Ms/s Nyquist rate**
- **Linear to "numerical noise"**
- **Power dissipation: 26 mW**
  - 11 mW analog circuitry
  - 15 mW digital circuitry
- **Chip back from fab Jan '00**

Simulation results of first integrator

DC Gain	A_{vo}	>600
3dB frequency	f_{3dB}	> 600 MHz
Phase margin	ϕ_m	> 65 deg
Differential Slew Rate		> 1000 V/μs
Sampling capacitance	C_{samp1}	100 fF
Power dissipation		< 3.2 mW

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