T Flip-Flop

The T-type flip-flop is simply a JK flip-flop with the J & K connections connected to logic 1. The output Q will then change state on either a leading edge or a trailing edge, which will result in a waveform with a frequency one half of the applied clock.

Figure **1** Shows the circuit of a simple J-K Flip-flop circuit to form a T-type Flip-flop using NAND gates.

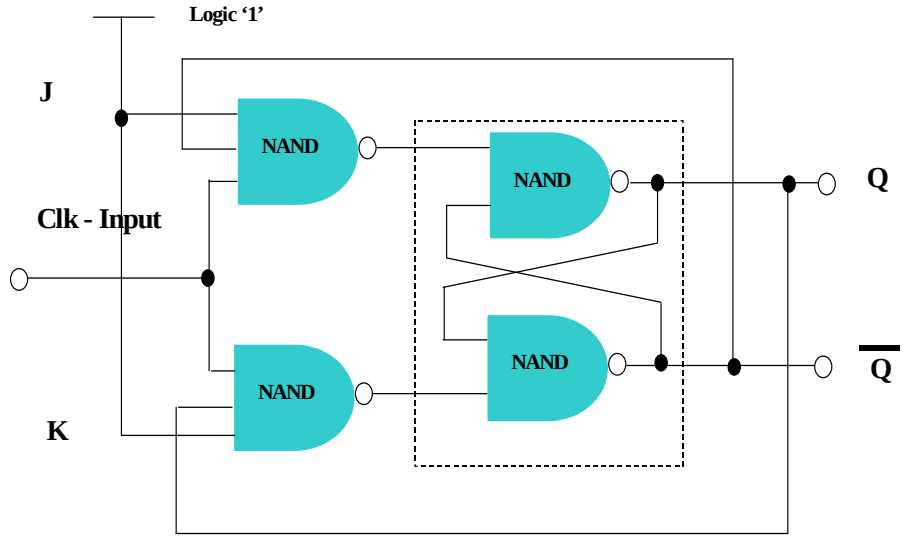

Figure 1 Modified J-K flip-flop with J & K inputs connected to logic '1' to form a T-type Flip-Flop (or toggle latch). The outputs will change on either the leading or trailing edge of the clock to give an output frequency of clk/2.

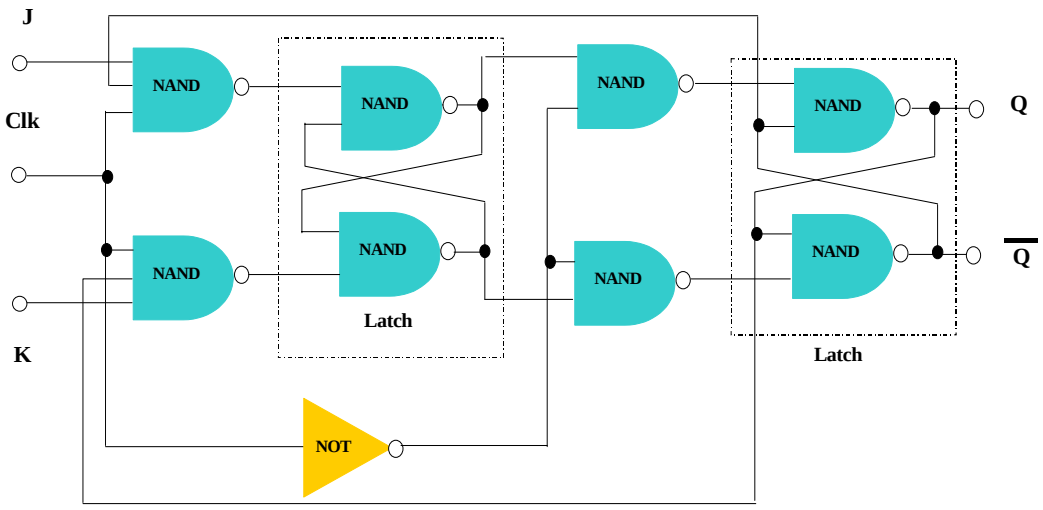

Figure 2 Improved T-type flip-flop with a master-slave latch to eliminate indeterminate logic states.

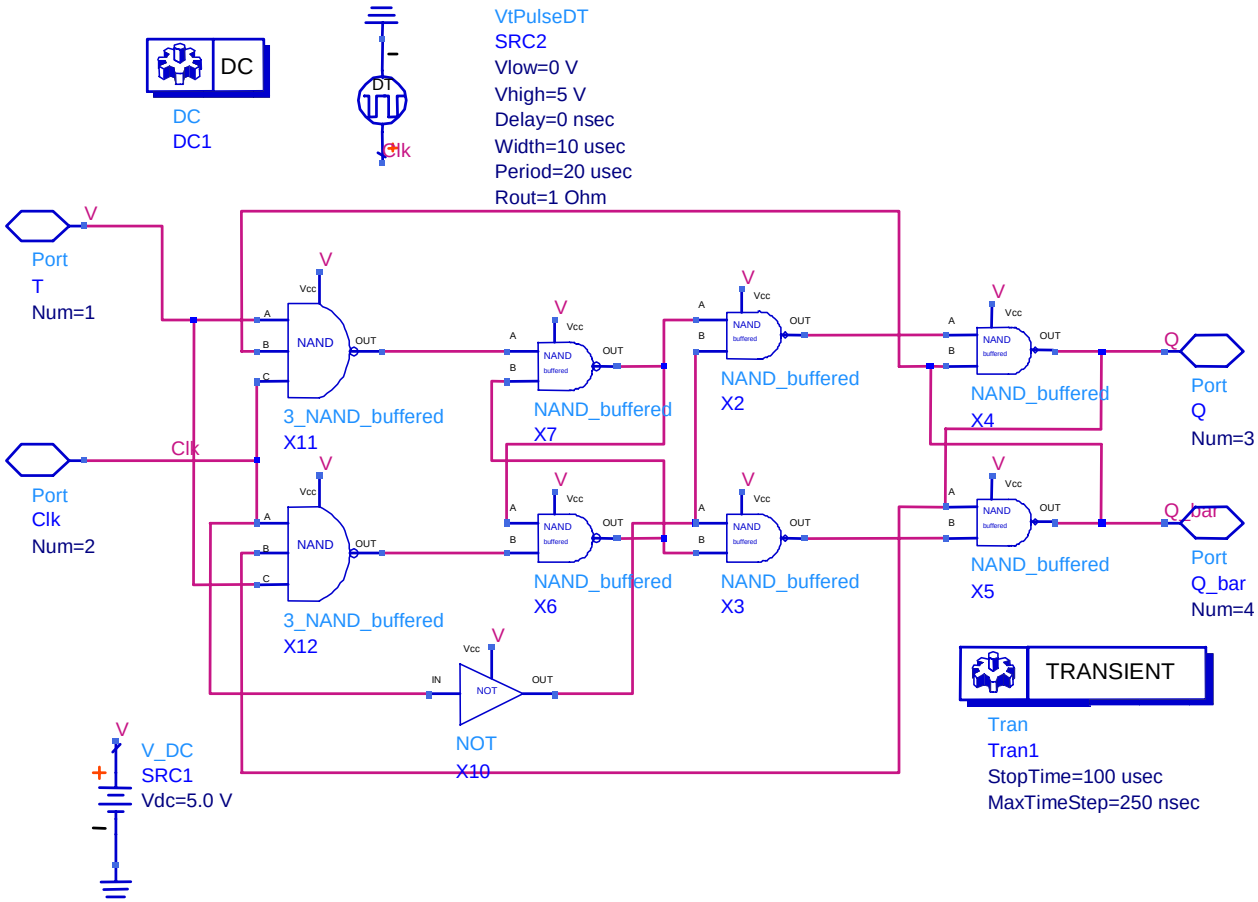

Figure 3 Master-Slave T-type Flip-flop ADS Transient simulation. The input waveform (Clk) is at 50KHz. The three input NAND gate is made by using 6 CMOS devices (Three N-types in series and three P-types in parallel).

D-type Flip-flop using 0.8um CMOS devices

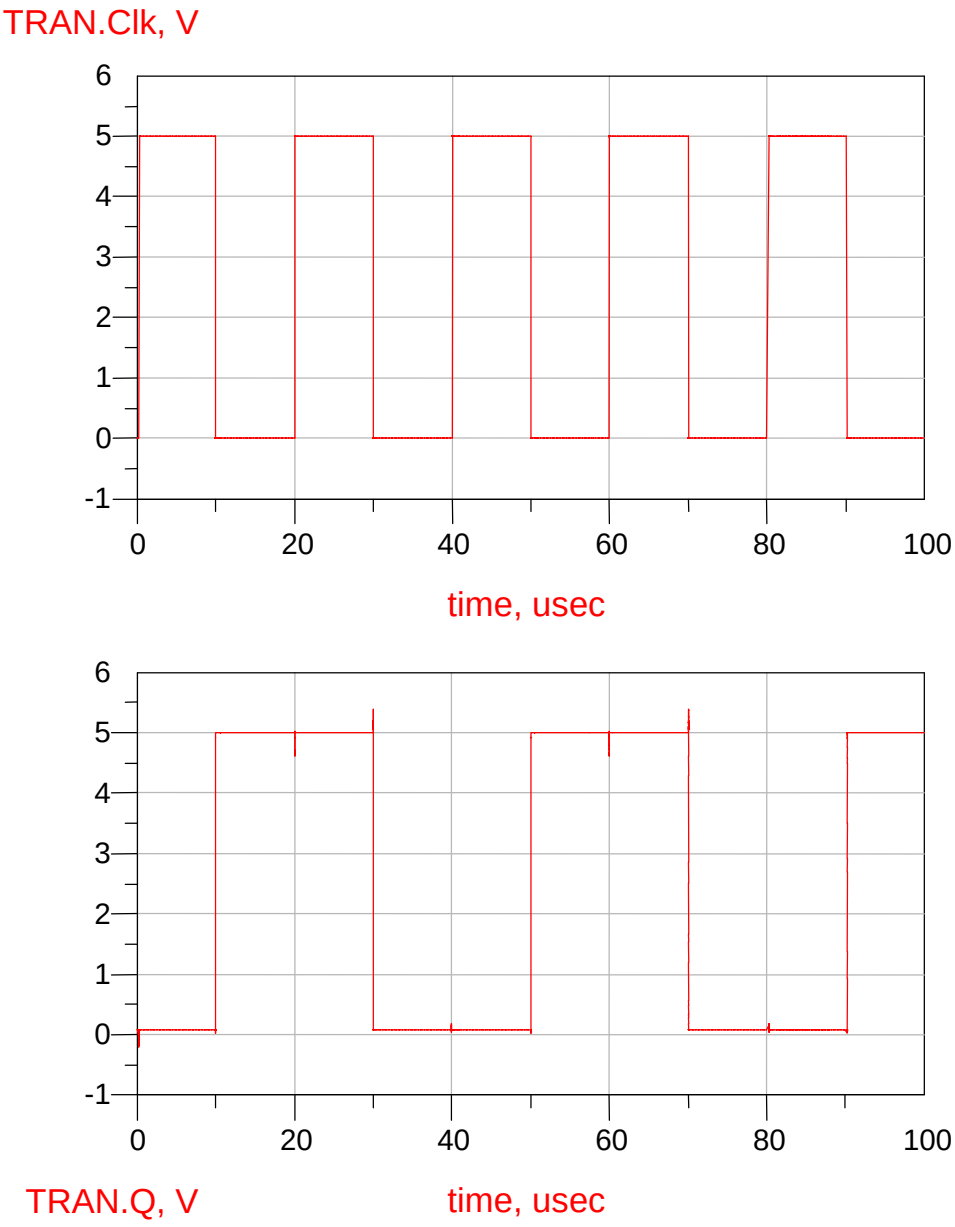

Figure 4 Simulation result from the ADS simulation of a Master-slave T-type flip-flop shown in Figure 3