ECE1352:
Analog Circuit Design

Term Paper
Integrated Smart Power IGBT Drivers

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November 15, 2002

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1. Introduction

The "System-On-a-Chip" concept that was born in the VLSI era has recently been applied to Power Electronics. Advanced processes such as BCD (Bipolar-CMOS-DMOS) from ST Microelectronics have allowed the integration of power devices and control circuitry. These so called "Smart Power ICs" (PICs) are one of the main driving forces in the miniaturization of power-hungry mobile applications. With the growing demand for mobile capability, the market for PICs is expected to increase from $17.7 Billion in 2000 to $26.8 Billion by 2005 [1]. Figure 1 shows a typical PIC. PICs have also been used in a wide variety of high-power applications such as:

- Electric Power Transmission
- Electric Trains
- Automotive
- UPS Power Supplies
- Motor Control
- Switching Power Supplies
- Household Appliances

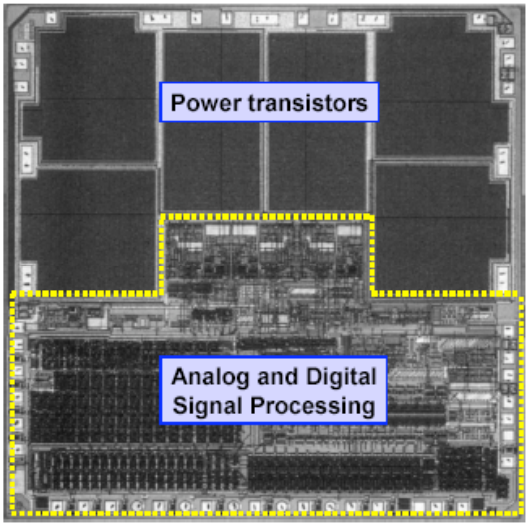


Figure 1: Industrial PIC (courtesy of W.T Ng)

Medium/High-power applications (>100W) still rely on discrete power transistors to carry current. In this case, PICs are used to drive the power devices while providing a wide range of protection and diagnostic features. This paper focuses on integrated gate-drivers for medium/high-power applications. A gate-driver IC is primarily an interface between a logic-level signal and a high-power switch module (see Figure 2). Gate-driver PIC development is fueled by the need to:

- Increase system reliability by decreasing the parts count
- Implement high-precision gate timing, which is impossible for discrete solutions due to mismatch
- Decrease the wiring requirements for multi-drive applications (motors on a multi-axis robot can be controlled with a single digital bus if the gate-drivers are integrated with the motors)
- Increase the switching frequency by eliminating parasitics present in a discrete
- Decrease the overall cost of power systems

- Include advanced protection features (over voltage/current etc.) which require the gate-driver to be mounted closed to the power switch

The following section elaborates on the gate-driver concept. The Insulated Gate Bipolar Transistor (IGBT) is the preferred power switch for high power applications. This paper will focus on two specific gate-driver properties that are more relevant to analog IC design (in accordance to the course material):

1. Gate Voltage Drive
2. High-side Supply Isolation

In each case, traditional and state-of-the art implementations are outlined and compared.

1.1 Gate-Driver Description

Figure 3 shows the ideal waveform for the typical half-bridge DC/DC converter of Figure 2. The output is switched between V_{BUS} and ground once every switching period V_{BUS} [2] and therefore the DC output can be expressed as:

$$V_{o\_DC} = \frac{1}{T_S}\int_0^{T_S} v_O(t)\cdot dt$$

$$= \frac{T_{ON}}{T_{ON}+T_{OFF}} V_{BUS} = D\cdot V_{BUS}$$

where D is the duty ratio. The waveform of Figure 3 is obtained by switching the gates of M_1 and M_2 in a non-overlapping complementary fashion as shown in Figure 2.

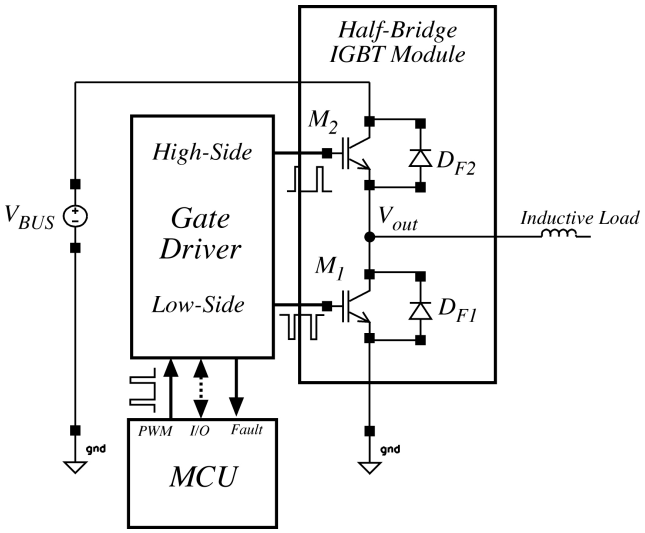


Figure 2: IGBT half-bridge

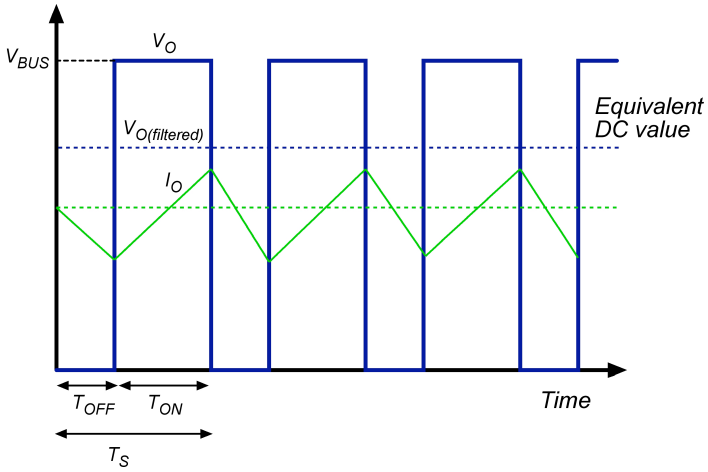


Figure 3: Switching waveforms for IGBT half-bridge

Designers have recently been striving to integrate the gate-driver with the power switches to achieve minimum cost and maximum reliability. This applies mainly to MOSFET switches in relatively low-power applications (<100W). This paper is concerned with high power applications where the power switches are isolated from the gate-driver circuitry. The gate-driver block in Figure 2 is required to provide the following functions:

- Provide sufficient current to charge/discharge the IGBT gate

- Protect IGBT module from dangerous operating conditions
- Ensure smooth current transition from high-side switch to low-side switch
- Level-shift digital PWM input to be compatible with IGBT Module

2. Gate Voltage Driving

Before outlining Gate Voltage Driving, an analysis of the IGBT structure and transient performance is required. The conventional IGBT structure is shown in Figure 4. The structure resembles a vertical Power MOSFET with the addition of the p+ injection layer near the drain terminal. This additional junction is also represented in the IGBT symbol of Figure 4.

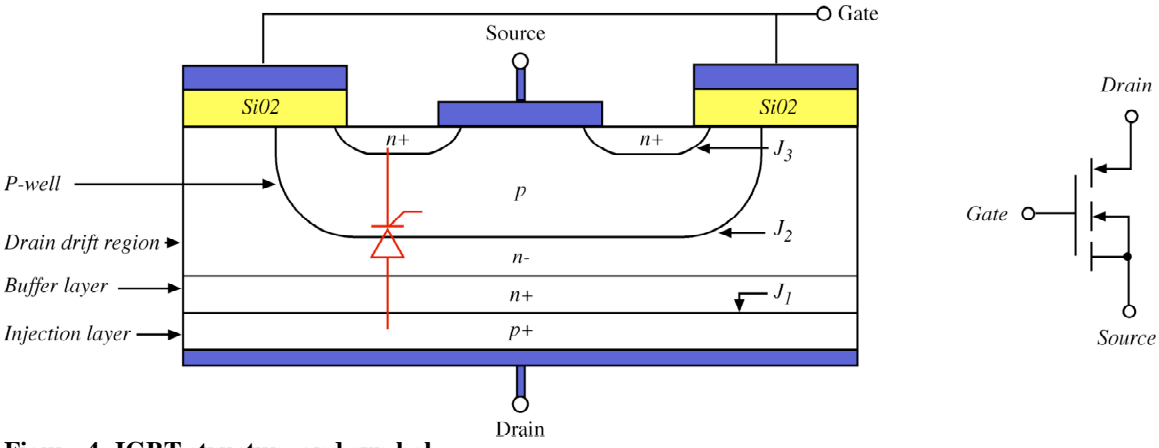


Figure 4: IGBT structure and symbol

2.1 IGBT Basic Operation

Figure 5 shows that the IGBT model has a Darlington configuration where the current is carried by the PNP and the NMOS. It practice, R_{BODY} is reduced to short the V_{BE} of the parasitic NPN. The PNP is made up of a P-well collector, a n- drift base and a p+ emitter.

The PNP base width is larger than conventional BJTs and therefore α_F is quite low. In fact, contrary to traditional Darlingtons, the NMOS "driver" carries the majority of the current. This ensures that the parasitic thyristor stays off. The purpose of the PNP is to modulate the conductivity of the drain by minority carrier injection. This reduces the IGBT's on-state losses. During on-state operation, the gate voltage is sufficiently high to induce a channel between the n+ source and the n- drift region. The drain current causes hole injection from J_1 into the n- region. The on-state voltage has three components [2]:

$$V_{DS\_ON} = V_{J1} + V_{DRIFT} + I_D R_C$$

where V_{DRIFT} is the voltage dropped across R_{DRIFT}, I_D is the drain current, R_C is the channel resistance. V_{J1} remains approximately constant (≈ 0.7V). The advantage of the IGBT is the low value of V_{DRIFT} compared to power MOSFETs. This reduction is due to the conductivity modulation of the n- drift region by the vertical PNP. The channel drop, I_D R_C is also present in MOSFETs.

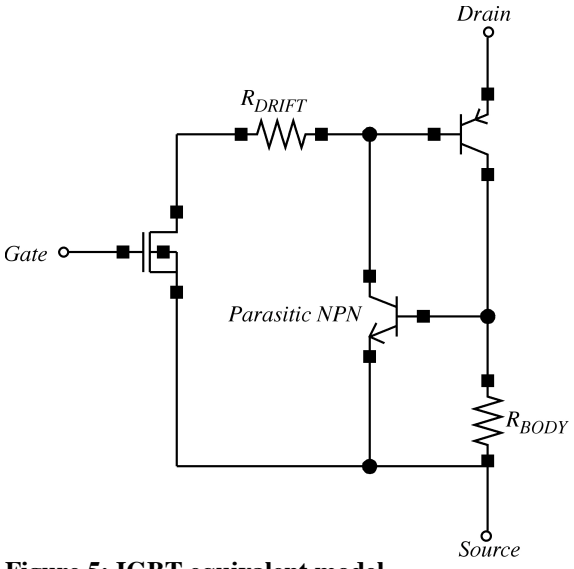


Figure 5: IGBT equivalent model

2.2 Breakdown/Blocking Considerations

The n+ buffer layer in Figure 4 is not mandatory for IGBT operation. Devices with this additional layer are termed "Punch-through" (PT) while others are called "Non-punch-through" (NPT). If the gate-emitter voltage (V_{DRIFT}) is below threshold, the MOSFET channel disappears and V_{DS} is supported across J_2. In a NPT device, the n- drift layer must be made large enough to support the n- depletion region. The n- thickness can be significantly reduced in PT devices by inserting the n+ buffer, which prevents the extension of the n- depletion region into the p+ drain [2]. The reduced n- thickness gives lower on-state voltage (and losses) but the PT design loses the ability to block reverse voltages (this is only a real disadvantage in AC applications).

The choice between PT and NPT IGBTs depends on the desired voltage drop and performance criteria. At high voltage ratings (≥2500V), NPT devices have lower overall

losses while PT devices are more desirable at lower voltage ratings. As discussed in the following section, the depth of the n- drift layer determines IGBT turn-off time. When the gate drive is removed, the n- region contains a relatively high concentration of minority carriers. If these carriers are not removed with a negative voltage, they slowly disappear by the recombination process. This results in an undesirable tail current. The tail current can be reduced by reducing the n- depth, at the cost of lower breakdown voltage. In practice, electron irradiation of the IGBT is used to control the n- carrier lifetime [2].

2.3 IGBT Transient Performance

The design of modern gate-drive circuits requires a solid understanding of IGBT switching characteristics and waveforms. The following section provides a condensed description of IGBT transient performance. This description outlines design issues and provides motivation for modern gate-drive circuits.

Figure 6 shows a representative half-bridge circuit. The analysis will deal with the low-side IGBT M_1. A similar discussion applies to M_2 but the required level-shifting complicates the analysis. A simple gate-drive circuit is depicted in Figure 6. The gate is driven by an ideal pulse-generator through a resistor. For reasons that will become obvious, a separate charging resistance is required for turn-on and turn-off. During turn-off, D_1 is forward biased and:

$$R_{off} = R_{on} \parallel R_{off'}$$

2.3.1 Turn-on Characteristic

IGBT manufacturers often specify the gate capacitance as a figure of merit. It is more important to look at the gate charge require to turn-on the device. This gate-charge can be used to estimate a constant charging current:

$$Q_{ON} = I_{charge} \cdot t$$

$$\Rightarrow I_{charge} = \frac{Q_{ON}}{t}$$

As an example, it would take 0.75A to provide 15nC of gate charge in 20ns. In practice, the charge current is not constant but the equation gives a good approximation of the switching speed. The half-bridge circuit of Figure 6 is always used to drive a relatively large inductive load. For continuous current application, the load inductance is sufficient to maintain a nearly constant output current. Figure 7 shows the switching waveform for M_1 when V_G is switched on [3].

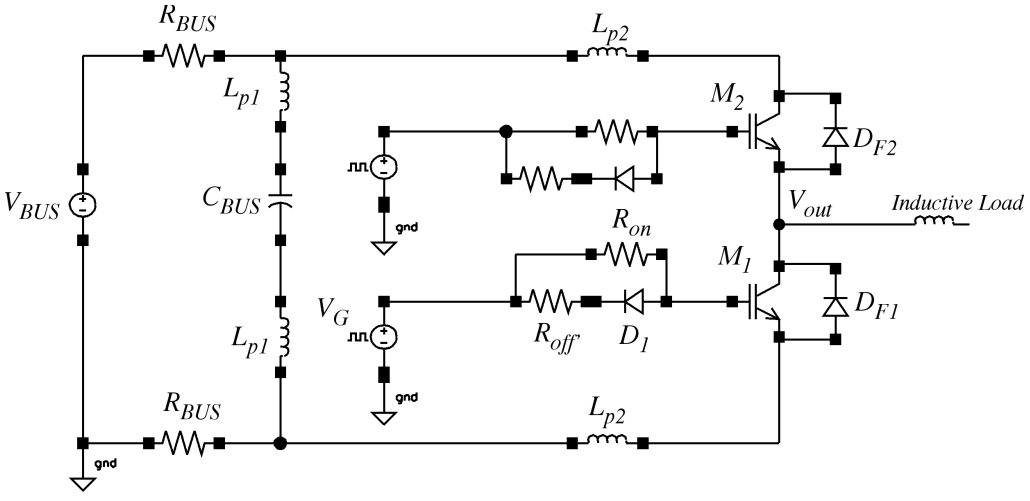


Figure 6: Representative IGBT gate-driver

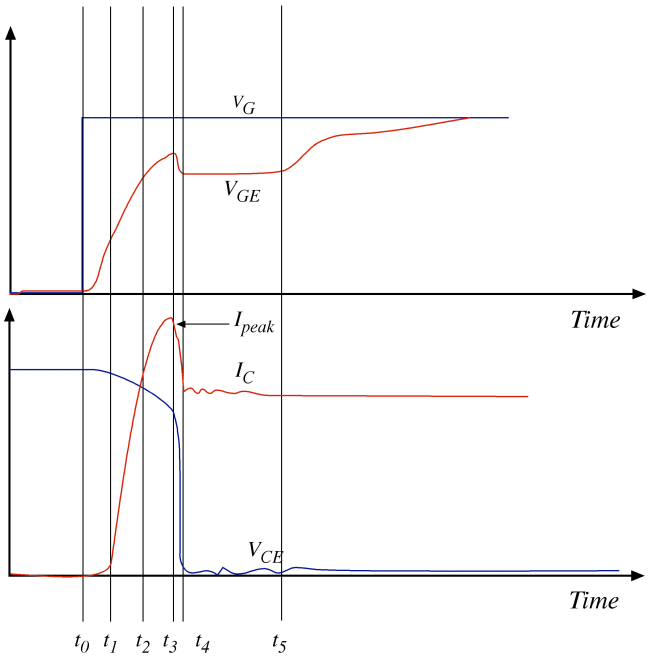


Figure 7: IGBT turn-on characteristic

The important parasitic capacitances of the IGBT are shown in Figure 8. When V_G turns on at t_0, the gate is capacitance C_{GE} is charged through R_{ON}. This causes V_{GE} to rise until it reaches the MOSFET threshold at t_2. At this point, I_C starts to increase and therefore V_{CE} drops. The drop of V_{CE} causes an initial drop in V_{GE} through the miller capacitance C_{CG} [4]. As mentioned previously, the output current is assumed to be approximately constant. This implies that when M_1 is off, the current is circulating through the freewheeling diode D_{F2}. As I_C increases, the output current is gradually transferred to M_1 until I_{DF2}=0. Since the diode is not ideal, it cannot support reverse voltage until the minority carriers are removed. This is referred to as reverse-recovery, which ends at t_4. The non-zero reverse recovery results in a high peak current. The large dV_{CE}/dt after t_3 causes the brief drop in V_{GE} due to C_{CG}. During t_4 to t_5 the gate drive is used to charge C_{CG} and therefore V_{GE} remains constant until C_{CG} is charged:

$$i_G = \frac{V_G - V_{GE}}{R_{on}} = C_{GC}\frac{\partial V_{CE}}{\partial t}$$

Additional voltage spiking occurs due to the parasitic inductance L_p in Figure 6.

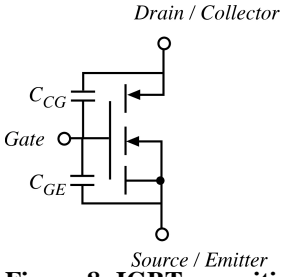


Figure 8: IGBT parasitic capacitances

2.3.2 Turn-off Characteristic

The turn off characteristic for a standard IGBT is shown in Figure 9 [3]. V_G is turned off at t_0, which causes C_{GE} to discharge through r_{off}. The output current is still carried through D_2 until $V_{CE} = V_{BUS}$ and D_2 is reverse biased. The constant V_{GE} between t_1 and t_2 is caused by the feedback coupling of dV_{CE}/dt into C_{GE} through C_{CG}. This is called the "turn-off delay" in [3]. At t_3, $V_{CE} = V_{BUS}$ and the current begins to commutate from M_1 to D_2 . The gradual decrease of I_C after is t_3 determined by the IGBT's physical properties (minority carrier lifetime) and is not affected by the gate drive. This discussion shows that the gate drive is much more critical in the IGBT turn-on situation. Nevertheless, R_{off} must be chosen carefully to meet dV/dT ratings and provide sufficient damping during reverse recovery.

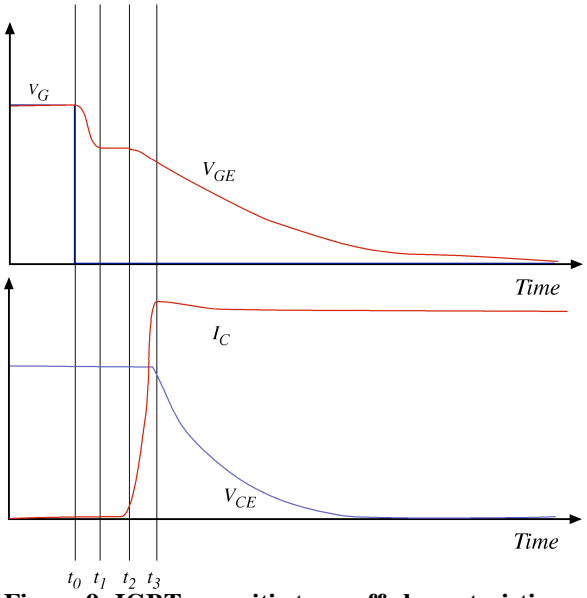


Figure 9: IGBT parasitic turn-off characteristic

2.3.3 Negative Gate Voltage

Applying a negative gate voltage to remove the minority carriers from the n- drift region can accelerate the IGBT turn-off mechanism. This is common practice in older Darlington BJT designs but is not usually required for IGBTs according to [5]. The negative gate-drive requirement is nearly impossible to achieve in monolithic gate-drivers. This has prompted most IGBT manufacturers such as International Rectifier to raise the IGBT threshold to eliminate the need for negative gate bias [6].

2.3.4 Losses and Gate Drive

The goal of an integrated driver is to maximize the switching frequency while satisfying SOA requirements and imposing acceptable energy losses. The dynamic switching losses occur twice every switching period: once during turn-on and once during turn-off. The energy lost during each period has two components. One component is the on-state losses

+ the off-stage losses (leakage) and the other is the dynamic switching loss shown in Figure 10. The dynamic component is the only component that can be optimized by the gate-drive circuit designer. The dissipated energy is calculated below:

$$E_{diss} = i_C(t) \cdot V_{CE}(t) \cdot dt$$

In one period, the dissipated energy is:

$$E_{diss} = \int_0^{t_{on}} i_C(t) \cdot V_{CE}(t) \cdot dt$$

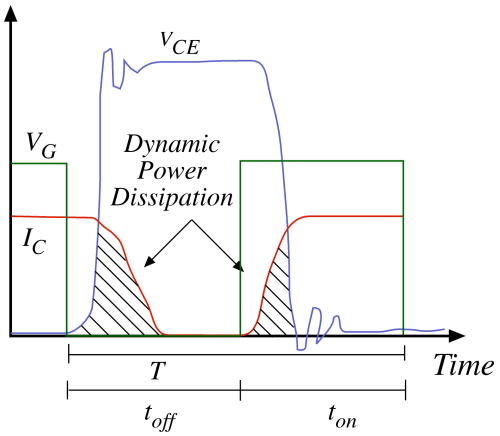


Figure 10: IGBT power dissipation

From the discussion on turn-on characteristics, increasing the gate voltage V_G speeds up the charging current commutation and drastically reduces E_{DISS}. The same effect can be achieved by reducing R_{GATE}. The gate resistance cannot be eliminated however because this would result in a low damped system with very high di/dt values. A high di/dt can destroy the IGBT or cause high voltage spikes due to parasitic inductance. In addition, it has been shown that the IGBT's maximum short-circuit tolerance time is reduced when using high V_G [4].

2.4 Classical Gate Drive Approach

The most common method of driving the IGBT gate is to use a source follower topology driven by a logic gate [5]. The IGBT is discharged using a common-source NPN. Figure 11 shows such a topology, which is used in a Motorola IGBT driver. The logic inputs to the AND gate are provided by a PWM and fault signals. R_{on} and R_{off} can be optimized separately. The two NPN transistors occupy the majority of the chip area, as they are required to supply instantaneous currents on the order of 1A.

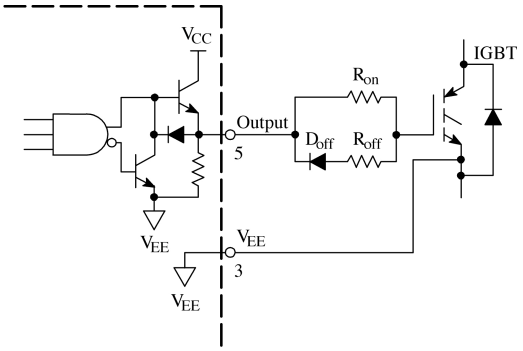


Figure 11: Typical gate-drive approach [8]

2.5 State-of-the-Art Gate Voltage Control

The switching characteristics can be improved by reducing the parasitic inductances in Figure 6 and by reducing the parasitic capacitances of Figure 8. These changes are not discussed since this paper focuses on IC design. Various advanced topologies have been proposed to improve IGBT switching characteristics. Three novel topologies will be briefly explained:

1. Improved turn-off
2. Linear current driver

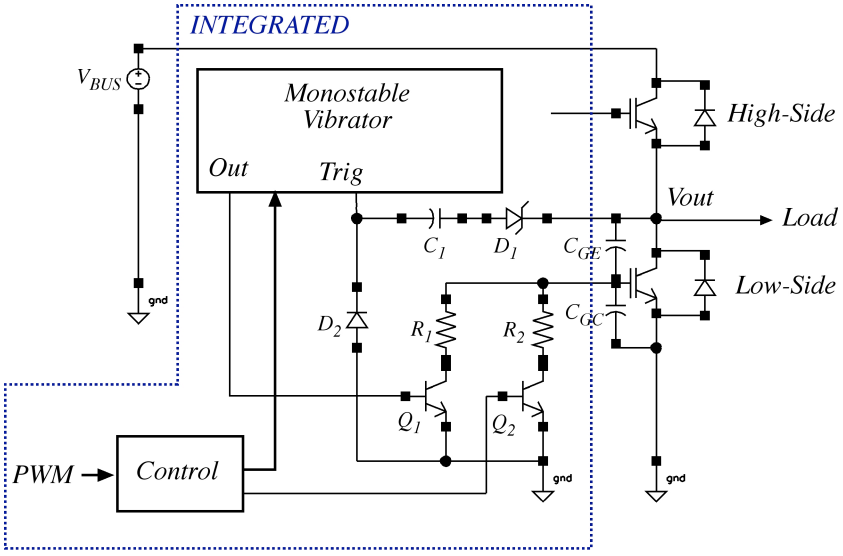
3. Variable gate resistance during turn-on

2.5.1 Improved Turn-off

An interesting topology proposed by [9] is shown in Figure 12. The experimental results from [9] are reproduced below. The discharge of the low-side switch is controlled as follows:

1. Q_1 and Q_2 are turned on which causes V_{out} (=V_{CE}) to rise rapidly
2. When V_{CE} reaches a preset value, zener D_1 turns on and the monostable vibrator is triggered.
3. The monostable vibrator momentarily turns off Q1. During this period C_{gate} is discharge through R_2 only ($R_2 >> R_1$) until I_C=0.

This circuit slows down the second part of the discharge interval to reduce the over-voltage. Since the initial d V_{CE}/dt is high, the energy consumption remains low (see Figure 12).



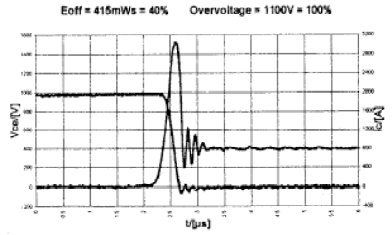


Fig. 4a: Conventional turn-off, high switching speed (R_g = 1,1 Ohm)

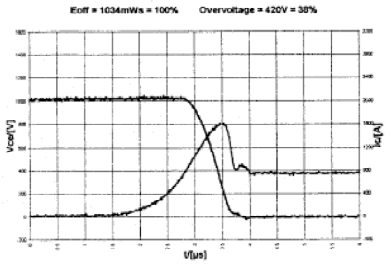


Fig. 4b: Conventional turn-off with low switching speed (R_g = 15 Ohm)

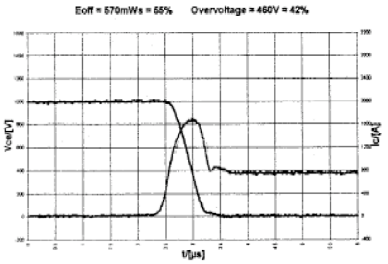


Fig. 4c: Turn-off with double-stage driver

Figure 12: Double stage driver topology and waveforms [9]

2.5.2 Linear Current Driver

Figure 13 shows a high-side gate-drive proposed by [10] to provide a linear charging current ($dI_{sw}/dt=k$). This eliminates the need for a gate resistance and minimizes over-voltage. Though the circuit was originally designed to drive a power MOSFET, the circuit could easily be modified for an IGBT. A simplified explanation is provided below (see [10] for more details).

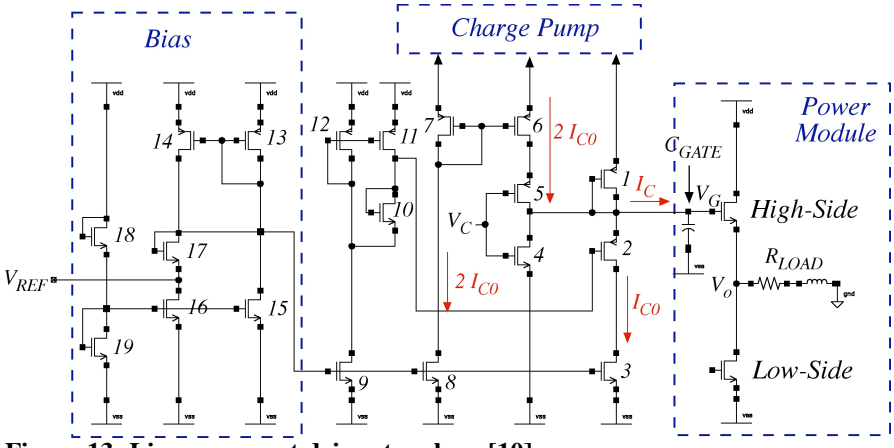


Figure 13: Linear current driver topology [10]

For $V_G < V_{DD} + V_{TN}$ the high-side switch M_{switch} is in saturation and therefore

$$i_{SW} = \mu_N C_{OX} (W/L)_{SW} (V_G - V_O - V_{TN})^2 \equiv k_{SW} (V_G - V_O - V_{TN})^2 \qquad (2.5.1)$$

Assume $\frac{\partial i_{SW}}{\partial t} = k_1$, then from (2.5.1)

$$V_G - V_O = V_{TN} + \sqrt{\frac{2k_1 t}{k_2}} \qquad (2.5.2)$$

The load constraint gives

$$V_O = R_L i_{SW} + L_L \frac{\partial i_{SW}}{\partial t} \qquad (2.5.3)$$
$$\Rightarrow V_O = R_L k_1 t + L_L k_1$$

From (x.2),

$$V_G = R_L k_1 t + L_L k_1 + V_{TN} + \sqrt{\frac{2k_1 t}{k_2}} \qquad (2.5.4)$$

and since $i_C = C_{gate} \frac{\partial V_G}{\partial t}$,

$$i_C = C_{gate} R_L k_1 + C_{gate} \sqrt{\frac{k_1}{2k_2 t}} \equiv 2I_{C0} + C_{gate} \sqrt{\frac{k_1}{2k_2 t}} \qquad (2.5.5)$$

When $V_G > V_{DD} + V_{TN}$ the high-side switch enters the triode and the analysis in [10] shows that the linear relationship can be maintained for:

$$i_C = I_{C0} \qquad (2.5.6)$$

When charge-up is desired, a control signal brings V_C to '0'. (2.5.5) is satisfied by M_6 which outputs $2I_{C0}$ and M_1, which has the $\sqrt{\frac{1}{t}}$ relationship in (2.5.5). M_2 is off until $V_G > V_{DD} + V_{TN}$ at which point it conducts I_{C0}. At this point, $I_C = 2I_{C0} - I_{C0} - I_{M_1} - I_{C0}$ and (2.5.6) is satisfied. M_{10}-M_{12} ensure that M_2 turns on when M_{switch} enters the triode region.

This circuit drastically improves the turn-characteristic by reducing the over-voltage in Figure 7, and eliminates the need for a gate resistance.

2.5.3 Variable Gate Resistance During Turn-On

The authors of [11] have developed a novel gate driver that has been successfully implemented in a Japanese high-speed electric train. The topology of Figure 14 actually reduces the gate resistance when a high dI_C/dt is detected. This is achieved using two mechanisms; dI_C/dt detection and resistance switching.

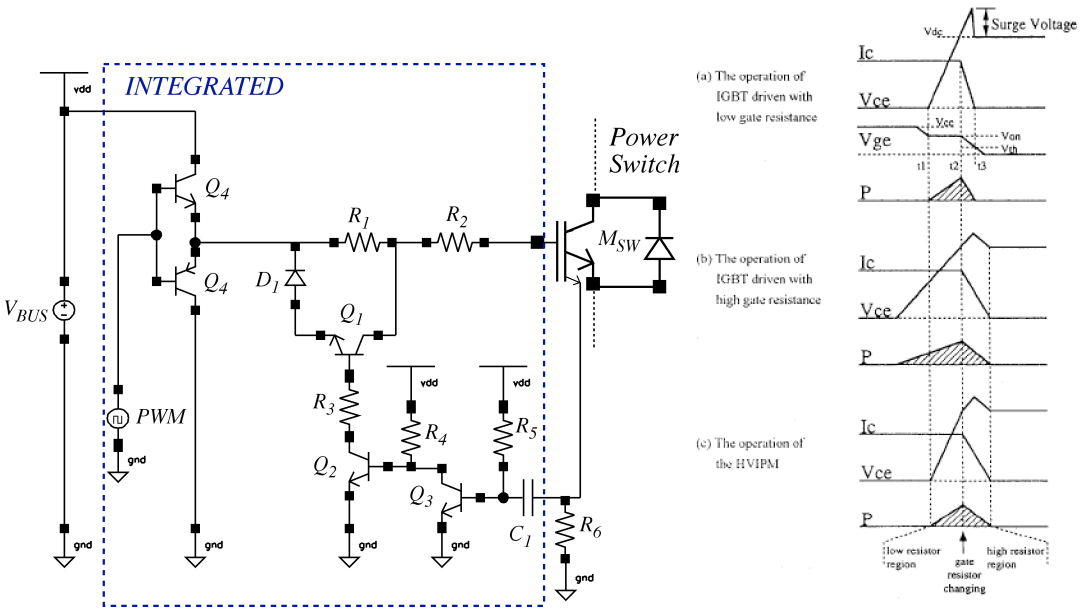


Figure 14: Variable gate resistance topology and theoretical waveforms

dI_C/dt Detection

Q_3 is biased *on* using R_4 and R_5. M_{SW} has an additional emitter used for current sensing (similar to popular *senseFET*™ technology). C_1 and R_6 form a filter that turns off Q_3 during excessive dI_C/dt.

Resistance Switching

During excessive dI_C/dt, Q_2 turns on which turns Q_1 off, resulting in a higher gate resistance (R_1+ R_2). The ideal waveforms of Figure 14 show how the circuit gives a better trade-off between over-voltage and switching speed.

3. High-Side Supply Generation

A closer look at Figure 2 shows why a specialized supply is required for the high-side IGBT. Since V_{OUT} switches between ground and V_{BUS}, the high-side IGBT's gate must be raised above V_{BUS} to main a sufficient V_{GS}. This section examines the traditional and state-of-the-art implementations for high-side supply generation.

3.1 Traditional Implementation

Before the advent of smart-power ICs, discrete drivers often used a separate supply generated using isolating pulse transformers. This bulky approach was soon replaced by partially integrated charge pump/ bootstrap circuits, which are widely used. The block diagram of a commercial gate-driver from *Linear Technologies* [12] is shown in Figure 15. The IC requires an external bootstrap diode and capacitor. The floating supply is created by injecting charge into the bootstrap capacitor while pin 13 is low. The LT1158 uses a 500kHz oscillator for this purpose. The zener diode clamps the high-side supply 15V above the high-side source to provide sufficient gate drive. The main limitation of this approach is that the bootstrap capacitor can be discharged if the high-side switch is off for an extended period (this occurs in brushless-DC motor applications). A solution to this problem is included in the next section.

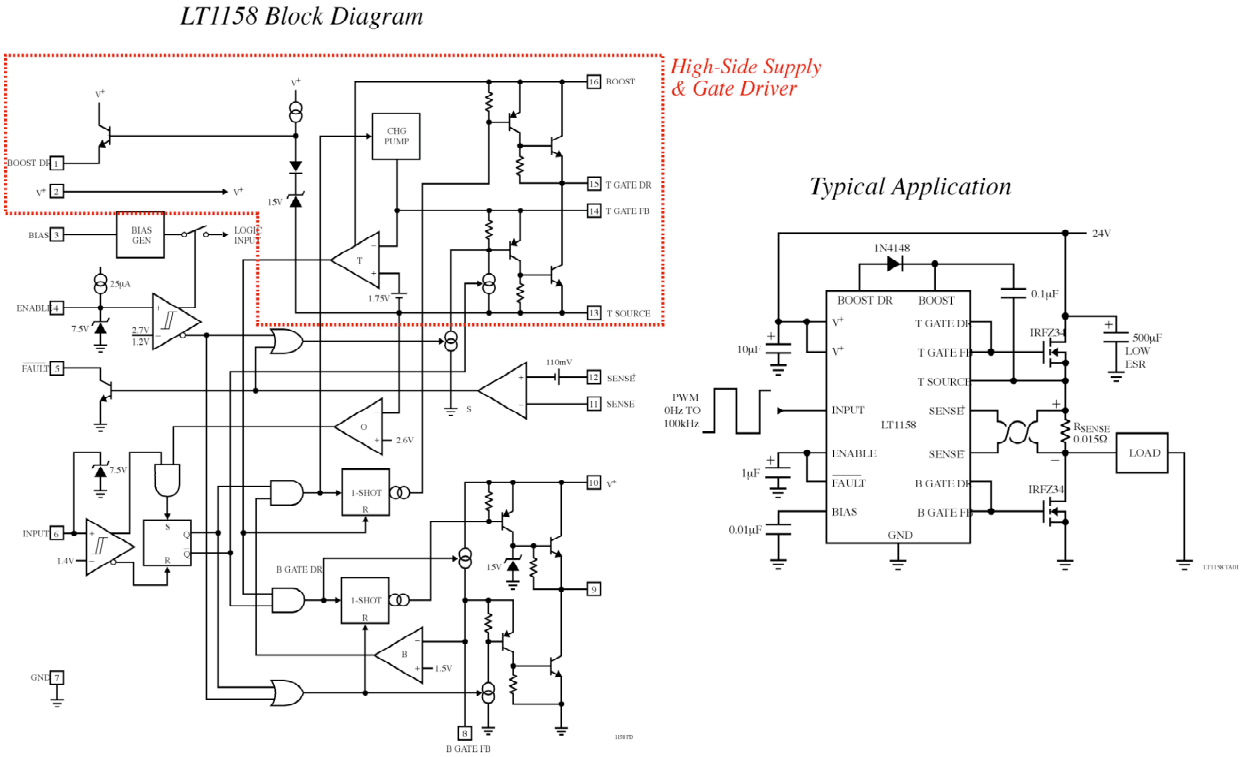


Figure 15: LT1158 Block diagram and typical application [12]

3.2 State-of-The-Art High-Side Supply

A novel charge pump topology has been devised by [13] to maintain a fixed high-side gate drive voltage regardless of the switching pattern. Figure 16 shows the topology, which is suitable for integration. The three modes of operation are shown in Figure 16.

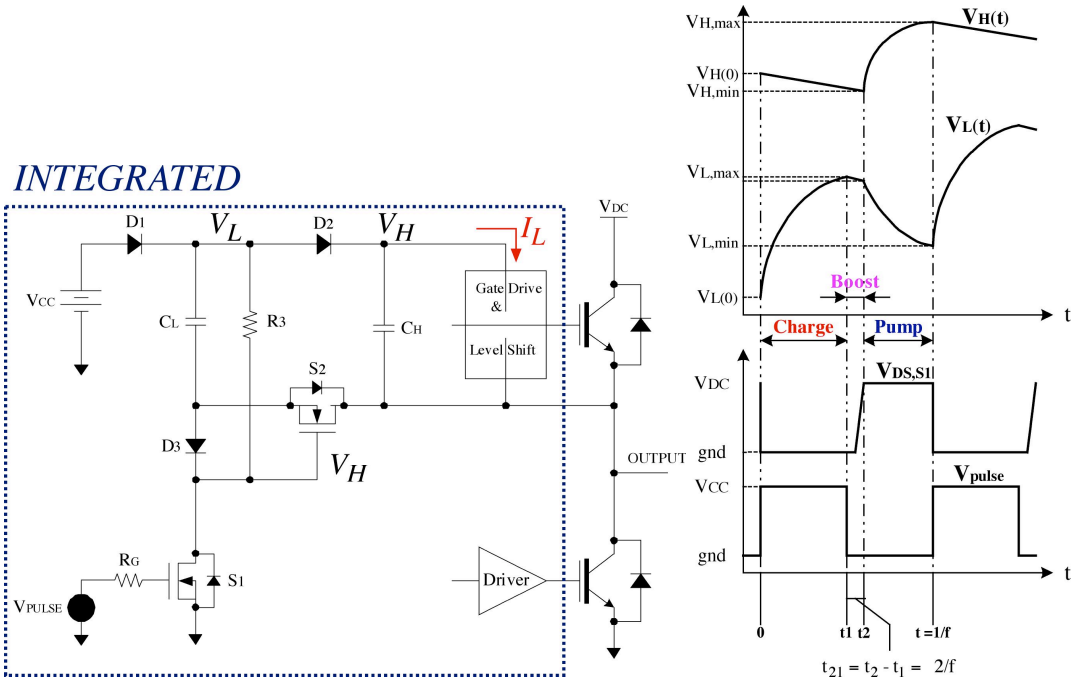


Figure 15 : Novel charge-pump topology and theoretical waveforms

1. Charge Mode

S_1 is turned on which shorts V_{GS2}. The charge-pump capacitor C_L is charged by V_{CC} through D_1 and D_3.

2. Boost Mode

When S_1 is switched off, D_3 and D_1 turn off and M_2's gate is gradually charged by C_L through R_3. When $V_{GS} > V_{TN}$, S_2 turns on. Notice that if $C_{gate} << C_L$, V_L stays approximately constant during this interval.

3. Pump Mode

Pump mode is initiated by the turn-on of S_2. S_2 transfers charge from C_L to C_H , which serves as the source-referenced high-side supply. Pump mode ends when S_1 is turned on. The following calculations are derived in [13]

During Charge mode,

$$v_L(t) = v_L(0) + \left[V_{L,MAX} - v_L(0)\right]\left(1 - e^{-\frac{t}{R_{EQ} \cdot C_L}}\right) \tag{3.2.1}$$

where $R_{EQ} = r_{D1} + r_{D3} + r_{DS1}$

During boost mode,

$$V_H(t) = V_H(0) - \frac{I_L}{C_H} \cdot t \tag{3.2.2}$$

During pump mode,

$$V_H(t) = V_H(0) + \frac{C_L V'_L(0) + C_H V_H(0)}{C_L + C_H}\left(1 - e^{-\frac{t}{\tau}}\right) - \frac{R_{EQ2} C_L^2 I_L}{\left(C_L + C_H\right)^2}\left(1 - e^{-\frac{t}{\tau}}\right) - \frac{I_L}{C_L + C_H} t \tag{3.2.3}$$

where $$\tau = \frac{1}{R_{EQ2}} \cdot \frac{C_L + C_H}{C_L \cdot C_H} \tag{3.2.4}$$

$$R_{EQ2} = r_{D2} + r_{DS2} \tag{3.2.5}$$

$$V'_L(0) = V_L(0) - V_{D2} \tag{3.2.6}$$

(3.2.3) assumes that the high-side drive draws a constant current I_L. Under steady-state conditions (3.2.2) and (3.2.3) give

$$V_{H,\max} = V_{CC} - V_{CC} - V_{CC} - V_{CC} - \frac{I_L R_{EQ2}}{1 - \delta_1 - \delta_2} \tag{3.2.7}$$
$$V_{H,\min} = V_{H,\max} - \Delta V_H$$

Where the charge-pump ripple is simply given by

$$\Delta V_H = \frac{I_L}{C_H \cdot f}(\delta_1 + \delta_2) \tag{3.2.8}$$

δ_1 is the duty ratio of the S_1 pulse while $\frac{\delta_2}{f_{PULSE}}$ is the time required for S_2 to turn on after S_1 is turned off. δ_2 is given by:

$$\square_2 = f_{PULSE} \cdot \left[R_3 C_{EQ2} \cdot \ln \frac{V_{CC} \square V_{D1} \square V_{D2}}{V_{CC} \square V_{D1} \square 2V_{D2} \square V_{TH} \square g_{m2}/I_L} + \frac{V_{CC} R_3 C_{GD}}{V_{L(0)} \square V_{TH} \square g_{m2}/I_L} \right] \quad (3.2.9)$$

The experimental results of [13] confirm the merit of this new topology for integrated gate-drivers with no restrictions on high-side switching patterns.

4. Future Challenges and Conclusions

The design of modern smart PICs requires knowledge in Analog/Digital and Power Electronics. This paper has focused on analog design issues relating to gate voltage control and high-side supply generation.

Efficient switching control has been demonstrated by using a variable gate-resistance topology during turn-on and turn off. This allows a high switching-speed while minimizing harmful voltage/current transients. One of the major problems with today's gate-drivers is the lack of versatility. A more advanced driver may be able to auto-calibrate the switching characteristics according to the particular device. This could be achieved by measuring the power switch's I-V curve during a calibration mode. This adaptive concept would give optimal performance for different IGBT sizes.

This paper also showed that a high-side supply can be achieved using a novel charge-pump technique. Most gate-driver charge pumps are not fully integrated because of the large boost capacitor requirement. Future designs may be able to achieve full integration by increasing the charge-pump frequency while maintaining low losses. A major challenge for future designs is the high voltage requirements on the high-side driver.

Processing improvements are yielding IGBTs with increasing dv/dt and di/dt ratings. Designing a PIC that handles sensitive analog and digital signals under these harsh operating conditions is becoming increasingly difficult. The future goal is to create so called “bullet-proof” gate-drivers, where the protection circuitry is so sophisticated that it is almost impossible to damage the power device. The gate-drivers of tomorrow will drastically reduce the cost and improve the efficiency of Power Electronic Systems.

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