Dual Motor Bidirectional Electronic Speed Control

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1.0 Introduction

This document describes an electronic speed control designed to drive two DC motors from a 7.2 Volt battery pack to be controlled by a commercial multi channel model radio control system. Conceived for a tank-like vehicle, one motor drives the left side wheels or tracks and the other motor drives the right side. As it is shown here, there is a left-right steering input and a forward-backward throttle input, like would be used on a model car radio unit. It is designed using analog circuits rather than a micro-controller or FPGA to allow construction with ordinary breadboarding techniques and no specialized device programmers. It will require a good voltmeter and an oscilloscope to perform the initial checkout and calibration. After designing and testing this project, it became pretty obvious that discrete analog is a painful way to do this due to the high parts count and the somewhat involved setup and calibration procedure, but there is still value in having a controller that can be built with no exotic equipment. An additional feature of this design is that it can be built in several configurations due to the modularity of the design. It has been configured with separate right and left throttle controls like a bulldozer, and it has been set up with direct wired controls instead of the radio link. *Note: This is a work in progress and is evolving as work is done on this project.*

2.0 Theory of Operation

As shown in the schematics, there are 5 major blocks to this design:

- Radio Interface. This block converts the pulse width modulated signal from a standard commercial radio control system into two analog control voltages.
- Summing Section. This block converts the steering and throttle signals into control voltages for the right and left motor PWM generators.
- PWM Generator. Converts the control voltages from the previous stage into Pulse Width Modulated digital signals suitable for driving the power sections.
- Right and Left Power Sections. Contain the power FET's and associated gate drivers to convert digital control signals into motor drive power. The power sections include the delay generation logic although it is shown separately.
- Power Supplies. Not shown on their own pages, there is a 5 volt power supply for the electronics and an 18 volt power supply for the FET gate drives.

Neglecting the power supplies, the signal flow is pretty much as described by the sequence above. Each section will be described separately.

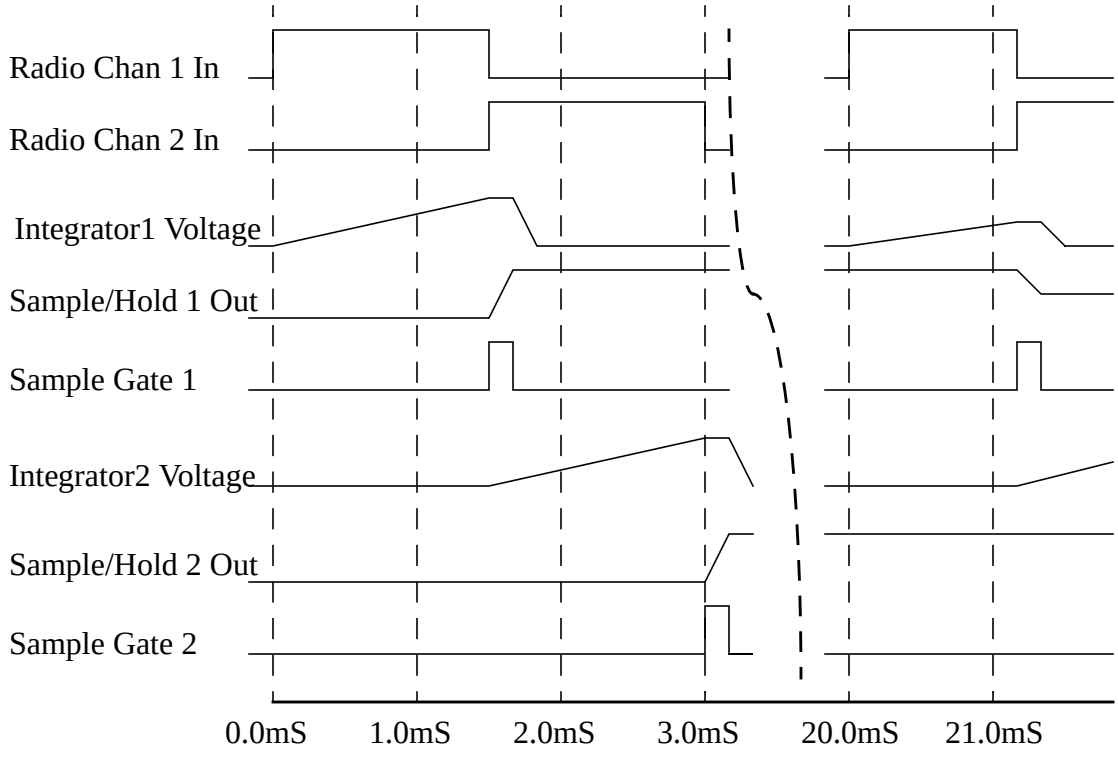
2.1 Radio Interface

Model radio control system since the 1970's have used a similar signal format for sending data from the receiver/decoder to the servos: a width modulated pulse. This pulse varies from slightly longer than one millisecond to slightly less than two milliseconds based on the position of the control stick or wheel. Mechanical center on the input device gives a 1.5 millisecond pulse. The repetition rate for the pulse is about 50 or 60 times per second. Some older radios output a negative going pulse, but the modern radios that I have seen (JR, Futaba, Hitech) all put out a positive going pulse. Since the pulses are transmitted serially, only one of the servo outputs from the receiver/decoder will be active at a time, although there is no significant time between adjacent channels in the datastream. The task of the radio interface circuit is to convert these pulses into a voltage that varies linearly with the input pulse width. There are two identical pulse width to voltage converter circuits in the radio interface section since there are two channels of radio input.

The pulse width to voltage converters work as follows: When the input pulse goes high, an integrator capacitor is allowed to charge at a constant rate until the input pulse goes low again. At the falling edge of the input pulse, an edge circuit generates a short pulse that opens the gate on a sample and hold circuit, saving the voltage present on the integrator capacitor. A short time later, the integrator capacitor is discharged in preparation for the next pulse. The sample and hold circuit holds it's voltage until the next pulse happens and the process is repeated. This approach provides a stable control voltage between pulse updates at the expense of slightly higher part count.

Details: A CMOS Exclusive OR gate (U2-A) is used at the input of the radio interface section to allow us to set this system up for positive or negative pulse radio systems. The output of CMOS gates goes very close to ground and 5 volts, which gives us a consistent large amplitude signal to work with later. When the output of U2-A is low, D2 is reverse biased or off. With D2 off, C3 discharges to the voltage set by the voltage divider (R10, R11, R13). Q5 is set up as an emitter follower so the voltage on C2 (the integrator capacitor) is about 0.6 volts above the voltage on C3. Current to charge C2 and keep Q5 forward biased comes from the constant current source composed of Q2, Q3, R8, R9, R14 and R15. As long as the output of U2-A stays low, the voltage in C2 stays near 0.6 volts. When the output of U2-A goes high to 5 volts, D2 conducts, charging C3 and turning off Q5. With Q5 off, C2 is allowed to charge from the constant current source until the falling edge of the input signal. At the falling edge of the input pulse, two things happen: first a short pulse is sent to the sample and hold by the edge circuit and D2 turns off again. With D2 off, C3 starts to discharge through R13 again. In a short time, the voltage on C3 will get low enough to turn Q5 on and start discharging the integrator capacitor again (C2) but the sample and hold gate will be off again before that happens. Transistor Q4 and R16 buffer the voltage on the integrator cap so that the sample and hold does not change the voltage appreciably. The sample and hold is made up of a CMOS Analog Transmission Gate, a capacitor, and an FET input OpAmp (U3-A, C4, U1-A). The gate on the Analog Transmission Gate (U1-A) is switched on for a short period of time and the storage capac-

itor (C4) stores the voltage that is present on the input pin (pin 1) and then the gate pin (pin 13) switches off, isolating the storage capacitor. Good quality, low leakage polystyrene capacitors should be used for the hold storage capacitors. The FET input OpAmp is connected to the storage capacitor as a unity gain buffer and has an extremely high input impedance so that it does not discharge the storage capacitor (C4) very rapidly. The output voltage on the OpAmp (U1-A) does not change appreciably between the input pulses arriving from the radio. This voltage is the steering control voltage that is passed on to the next stage. The resistors (R4, R6) are placed around U1-A so that some gain could be put in if needed. The edge circuit works by charging C1 through D1 and R1 while the input signal is high. When the input signal goes low, the base of Q1 is pulled down, turning it on. The voltage in C1 goes to the gate input of the Analog Transmission Gate and also discharges through R7 to ground. Since C1 is a fairly small capacitor (0.02uF) it gets discharged in a few microseconds through R7 (1k), resulting in a nice short sample time for the sample and hold circuit. As can be seen from the description, the longer the input pulse is high, the higher the output voltage from the OpAmp. This relationship is very linear due to the constant current source used to charge the integrator capacitor. When the input pulse is 1.5 milliseconds long, the output voltage should be about 2.5 volts. The Span Adjust pot (R15) and the Zero Adjust pot (R11) should be adjusted so that the output voltage swings between 1.5 volts and 3.5 volts as the control stick or wheel is moved from limit to limit.



PulseWidth to Voltage Conversion Signals

For the rest of the circuits operation, we are going to assume that neutralized controls correspond to 2.5 Volts, forward throttle or right steering input = higher voltage and backward throttle or left steering = lower voltage. Since 2.5 Volts is the neutral position, it will be assumed to be the “zero” in the Summing and PWM generation sections.

In order to protect the vehicle if the motor power is turned on before the radio transmitter, there is a circuit that shuts off the motors if there are no pulses from the radio for a period of time. The first part of that circuit is in the Radio Interface section. Incoming pulses from both the steering and the throttle channels charge capacitor C5 through XOR gate U2-C and diode D3. When the input signals are both inactive, D3 is reverse biased and off so C5 discharges through R17 to ground. When the voltage on C5 gets low enough, the voltage comparator U6-B on sheet 3 of the schematics switches high, shutting off the output driver IC's on sheets 5 and 6.

2.2 Summing Circuit

Since this controller is designed for controlling a tank-like vehicle, the motor control voltages are more complex than just the analog version of the input signals. In order to make a tank-like vehicle turn to the right, it is necessary to make the left tread drive forward and the right tread drive backward. If the vehicle is moving forward, the left tread needs to go forward faster and the right tread more slowly or even reverse slightly. Assuming the effective "zero" of 2.5 Volts being neglected here, in this situation the left motor control signal would be:

$$LeftMotorControlVoltage = ThrottleControlVoltage + SteeringControlVoltage$$

and the right motor control signal would be:

$$RightMotorControlVoltage = ThrottleControlVoltage - SteeringControlVoltage$$

This function gives a "rotate" effect that makes sense when the vehicle is going forward, but is opposite of what we want when the vehicle is backing up. When the vehicle is backing up, we will reverse the polarity of the steering signal so that when both treads are moving backwards at the same speed and we apply right steering, the left tread will now move faster in reverse and the right tread will now move more slowly in reverse.

Details: The steering control voltage comes in from the Radio Interface section and is routed to one of the Analog Transmission Gates (U3-C). It is also routed to an inverting OpAmp (U5-B) to make the reversed steering signal. The reversed steering signal is routed to another Analog Transmission Gate (U3-D). The outputs of both of these Analog Transmission Gates are tied together. The gate signals for these Analog Transmission Gates are controlled by a Voltage Comparator (U6-A) connected to the throttle control signal. The output of the comparator controls one of the gates directly and the other gate is controlled by the logical inversion of the comparator output, so that one or the other Analog Transmission Gate is always on. A reference voltage for the comparator is set with pot R45 which should be set so that the voltage on pin 4 of U5 is about 2.45 Volts. The logical inversion of the Comparator output is done with an XOR gate (U2-D) that we had left over from the input circuitry. The inverting OpAmp will need to have it's offset nulled, so with the steering control voltage at 2.5 Volts, set pot R41 so that the output pin (7 of U5) is at 2.5 Volts. We now have a throttle signal selected reversible steering signal to be added and subtracted with the throttle control voltage. Resistors R32, R33 and R34 form a summing junction for the steering signal and the throttle signal. This signal is buffered by OpAmp U4-B to provide the left motor control voltage. Our reversible steering signal is fed into another inverting OpAmp (U5-A) and then summed with the throttle signal in resistors

R35, R39 and R42 and then buffered by OpAmp U4-A to provide the right side motor control voltage. The inverting OpAmp U5-A also needs to have it's offsets zero'd with pot R43. Once again with the steering input at 2.5 Volts, set R43 so that U5 pin 1 is at 2.5 Volts. The two summing amplifiers give the following arithmetic results:

$$LeftMotorControlVoltage = \frac{ThrottleControlVoltage}{2} + \frac{(\pm SteeringControlVoltage)}{2}$$

and:

$$RightMotorControlVoltage = \frac{ThrottleControlVoltage}{2} - \frac{(\pm SteeringControlVoltage)}{2}$$

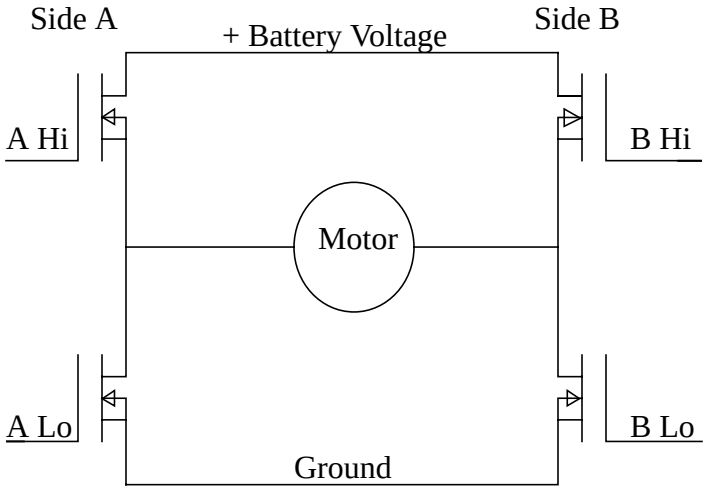
It can be seen from these two equations that these control voltages will have similar ranges as the two input control voltages. Since the incoming Voltages are divided by 2 in the final result, full right steering and full forward throttle will result in about 3.5 Volts on the left motor control voltage and full reverse throttle and full left steering will result in about 1.5 Volts on the right motor control voltage. The left motor control voltage is available on U4 pin 7 and the right motor control voltage is available on U4 pin 1 to send to the next stage.

2.3 PWM Generator

We now have a separate analog control voltage for each motor whose range is about 1.5 to 3.5 Volts with 2.5 Volts being the off value. In order to get good efficiency driving the motors, we will use PWM (Pulse Width Modulation) to control the effective voltage to each motor.

$$EffectivVoltage = Vbattery \times \frac{TimeOn}{TotalTime}$$

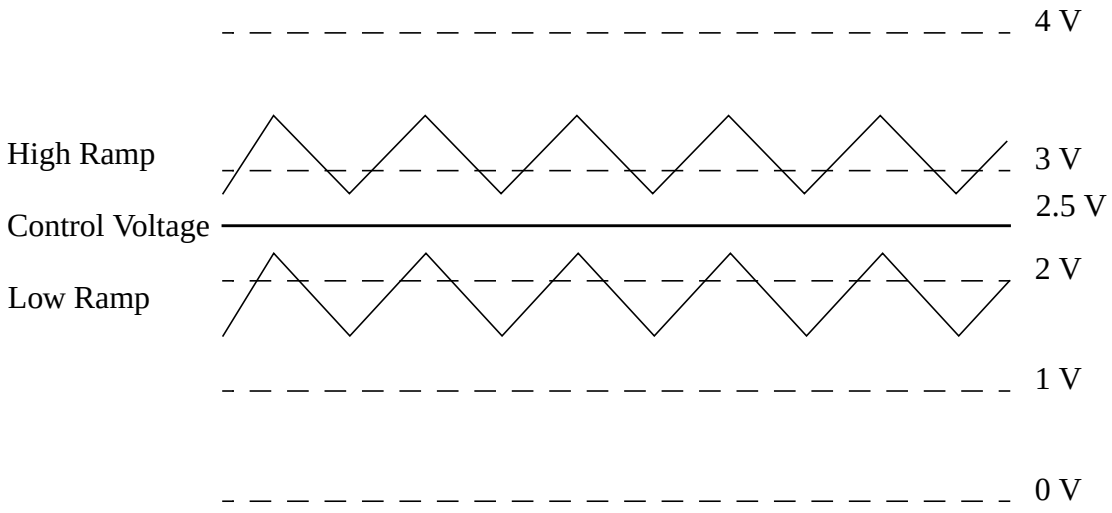
Since the motors must be able to run forward or backward, we will set the output transistors up in an H Bridge configuration. In this configuration, each side of the motor gets two transistors attached to it: one tied to the battery positive line and the other tied to ground. It



H Bridge Motor Drive Circuit

is obvious that both transistors on side A can not be on at the same time and the same applies to side B, so Side A Lo can be driven off of an inverted copy of Side A Hi and Side

B Hi can be driven off of an inverted copy of Side B Lo. This arrangement means that the high and low transistors can never be on at the same time (a very bad thing!) and we only have to generate two unique control signals per motor now. In order to run the motor forward, we will turn on the Side A Hi and the Side B Lo transistors. For reverse, we will turn on the Side B Hi and the Side A Lo transistors. To convert the analog control voltages for each motor into PWM H Bridge control signals, we will use two triangular waves and two Voltage Comparators per motor. Each Control Signal will go to both Voltage Comparators for that channel. One of the Comparators will get the high ramp signal as it's other input and the other Comparator will get the low ramp signal as it's other input. The output of the high ramp Comparator will drive the A side of the H Bridge and the output of the low ramp Comparator will drive the B side of the H Bridge. In the drawing below, the Control Voltage is at 2.5 Volts, between the two ramp signals. The Control Voltage is below the



PWM H Bridge Control Signal Generation

High Ramp and above the low ramp, so both sides of the bridge have their ground sides conducting, and the motor is turned off. If the Control Voltage were to rise a a small amount, it would soon be above small parts of the high ramp signal. The high side transistor on the A side of the bridge would turn on during those small parts of the wave and the low B side transistor is still on since the control voltage is all above the low ramp. Since the high side A transistor is only on for a very short amount of time out of the total, the motor is not driven very hard. If the Control voltage were to rise a lot, such as to 3.4 Volts, it would be above the high ramp almost all of the time so the high side A transistor would be on almost all of the time. Conversely, if the Control voltage were to drop a small amount below 2.5 volts, it would be below the top of the low ramp for a small amount of time, so the high B side transistor turns on and the low A side transistor stays on and the motor turns slowly in reverse. There are two of these circuits, one left and one right channel, both using the same two ramp signals.

Voltage Comparators are very sensitive to noise around their transition regions, so a technique called hysteresis is commonly used to reduce this problem. Hysteresis is a term that refers to causing the comparator to switch at one voltage when it is transitioning from a

low to a high output state and switching at a slightly higher voltage when transitioning from a high to a low output state. This difference may be only a few milliVolts, but it is enough to insure that the comparator makes a single clean transition when the two input voltages cross each other.

The triangular wave generator is built from a 555 IC, two switchable constant current sources and a timing capacitor. The standard 555 circuit provides an almost triangular wave as the voltage on the timing capacitor. It is actually an exponential up and down ramp because the capacitor is being charged and discharged through resistors. Replacing the resistors with constant current sources changes that into the triangular wave that we want to give us a linear output response to a linear input change. It is necessary to make the current sources switchable in order to charge and discharge through them. The current sources are Widlar Current Mirror's with an extra transistor added for switching them on and off.

Details: When the voltage on the ramp generator timing capacitor (C11) is less than 2/3 VCC, the discharge pin on the 555 (pin 7) is floating high, pulled up by R50. With this pin high, the discharge current source is turned off: transistor Q17 conducts, forcing the bases of the transistors in the current source (Q15, Q16) below their turn on voltage. The charging current source is turned on since it's shutoff transistor is not conducting. The current from transistor Q12's collector charges the timing capacitor (C11) until it's voltage reaches 2/3 VCC where the 555 IC drives it's discharge pin (pin 7) low. With the discharge pin low, the charging current source is switched off and the discharge current source is switched on, discharging the timing capacitor through the collector of Q15. When the voltage on the timing capacitor discharges to 1/3 VCC, the 555 IC turns off the discharge pin (pin 7) and the current sources will switch back to charging C11 again. This sequence is repeated continuously.

The triangular voltage signal on the timing capacitor is buffered through transistor Q14 operating as an emitter follower so that we don't effect the 555 IC's operation with things we do downstream. Potentiometer R63 is used to set the amplitude of the triangular waves we will use for the PWM generation. Both the upper and lower ramp signals should be the same amplitude. In order to shift the upper and lower ramp DC levels, they are AC coupled through capacitors C10 and C13. The new DC levels for the ramps are set with potentiometers R57 and R70. These two signals are ready for use in the voltage comparators in the PWM generators.

In order to put hysteresis in the comparators without risking crosstalk between the two channels, some liberties were taken with the comparator circuit configurations. Since the hysteresis is put in by modifying the signal at the positive input of the comparators, the ramp signals were routed into the negative input and the control voltage inputs were routed into the positive inputs. This resulted in the logical inversion of the Side B output signals. This is not a problem since we are generating an inverted copy of that signal in the output section anyway, but it is not obvious from looking at the comparator circuits. All of the voltage comparators are in a single package (U7) and are LM339's. Note that these comparators are open collector output parts and require a pullup resistor (R54, R59, R64, R69) for each output. The 2.2meg resistors from the outputs back to the positive inputs, in

conjunction with the 20k resistors are what provides the hysteresis. With these four comparators, we have logic level control signals for the left motor A and B sides of the H bridge and the right motor A and B sides of the H bridge. These logic level control signals are ready to go the output sections.

Tuning the PWM Generator involves some choices. It seems like full speed on the throttle control should be able to drive maximum speed on the motors, but with the steering signal added to this value, it would ask for more than full speed on one motor and slow the other motor down. Obviously asking for more than full speed will not make the motor go faster. This tuning arrangement causes some non-linearities in the steering control function, but allows the vehicle to travel at it's maximum speed. To get this style of tuning, remember that the summing section divided the throttle and steering inputs by two. Maximum throttle deflection provides +/-.5 Volts of deflection about the 2.5 Volt center on the two motor control signals, assuming that the input section provides +/- 1.0 Volts. With an oscilloscope, measure the triangle wave peak to peak amplitude at the wiper of potentiometer R63. Adjust R63 so that the peak to peak value is slightly less than 0.5 Volts, neglecting the DC component entirely. Now move the scope input to the HI-RAMP input on the comparator (pins 4 or 8 of U7) and adjust the UPPER OFFSET VOLTAGE potentiometer R57 until the bottom of the triangle wave is slightly above 2.5 Volts. Connect the scope input to the LO-RAMP input of the comparator (pins 6 or 10 of U7) and adjust the LOWER OFFSET VOLTAGE potentiometer R70 until the top of the triangle wave is slightly below 2.5 Volts. The separation of the bottom of the HI-RAMP and the top of the LO-RAMP signals is the neutral deadband on the controls. If it is set too small, the motors will never be truly off, and if it is set too large, the steering and throttle will not respond to small changes around the neutral position of the controls.

The other extreme of the PWM tuning would be to set the triangle wave amplitude to 1.0 Volts peak to peak, and set the offset voltages with the same technique previously described. This tuning approach gives the most linear steering response at all throttle settings at the cost of having the overall speed of the vehicle be half of it's maximum capability.

2.4 Output Sections

There are two identical Output Sections, one for the left motor and one for the right. Since two logically inverted control signals are required for each side of an H Bridge, the control signals generated in the PWM generation section are each fed to an inverter. We now have the required 4 control signals for two separate H bridges. Referring back to the drawing of the H bridge, you can see that if both transistors on one side of a bridge were turned on at the same time, we would have a direct short to ground. This problem is called shoot-through current and it is a bigger problem than might be expected. Large FET's like we want to drive our motors with have a lot of capacitance (7400pF for the ones I used) on their gate leads, so it is difficult to switch them on or off quickly. This switching delay makes it very easy to have both FET's on for a short period of time each time there is a transition from one FET conducting to the other. A LOT of power can go through in that time and it will heat up transistors and cook them very quickly if allowed to happen. For this reason there are delay circuits put in between the logic level control signals and the

actual FET Gate Drive IC inputs. These delays cause the gate turn on to be delayed a hundred nanoseconds or so and the gate turn off to be un-delayed, guaranteeing that we don't cook things with shoot-through current.

Electric motors have a large amount of inductance so that when you switch the current to them off rapidly (which is what PWM is all about) you get a large voltage spike. This voltage spike will turn on the body diode in the opposite transistor while it bleeds off the energy stored in the motor's inductance. By virtue of the way we are handling the gate control on the FET's, we will help get rid of this energy by turning the opposite FET on when we turn one off. This technique is called synchronous rectification. Having excessively long delays on the gate control hinder this effect, making the body diodes carry more of the load. After a lot of experimentation, I found that adding very fast diodes across the FET's helps to protect the FET's since the body diodes are fairly slow.

After the delay circuits, it is necessary to turn logic level signals into FET gate drive signals. The large amount of capacitance seen looking into the gate on a large FET makes this kind of a problem. The fact that this design uses 8 FET's adds to this problem. Initially, I tried to do this with discrete parts, but realized that adding a couple of parts to fix this problem and a couple of parts to fix that problem soon amounted to a bunch of parts! I punted and used the International Rectifier IR2110 half bridge gate driver chips. These little jewels are easy to use, work well and there is a high and a low side driver in each package.

FET's require a fairly high gate voltage to turn on solidly, around 10 volts between the gate and source terminals for most of the large ones. Our system is designed to run on a 7.2 Volt battery pack, so right away we have a problem. In our system, there is a separate power supply to generate this higher voltage (about 18 volts) for the gate drives. If this system ran on about 12 volts or higher, we could use a simpler way to get that elevated voltage. If this circuit is modified to run on 12 volts or so, look at the data sheets for the drive IC's (IR2110) and you can save yourself a few parts by using a bootstrap capacitor instead of the separate 18 volt power supply.

Details: Since there are two identical motor drive circuits, only one will be described. Inverter U10 is used as a buffer and an inverter. To isolate the comparators in the PWM generation section from the low impedance delay section, two inverters connected sequentially are used as a buffer or a single inverter is used where logical inversion is needed. Comparator U7 pin 2 provides the A side control signal. This control signal is routed to U10:A for control of the low side FET and U10:B and U10:C for the high side FET control signal. The output of U10:C charges capacitor C19 through resistor R78 and discharges C19 through diode D7 when the output goes low. Using the voltage on C19 as the input to the FET gate drive IC U11, this R/C/Diode arrangement provides a small delay for turning on the gate drive and almost instant turn off. A similar path is used on the low side gate signal with U10:A, R80, C23 and D9. Side B of the H bridge works similarly with the exception of the high side control signal is inverted and the low side is buffered for side B. The gate drive IC's have Schmidt trigger inputs so that they will provide consistent transition voltages and clean switching with the R/C delay outputs. The gate drive

IC's convert the logic level control signals from the delay circuits to the 0 to 18 volt high current signals required for fast switching on the power FET's.

In view of the amount of electrical noise in this part of the circuit, it is advisable to put a decoupling capacitor (.1uF or so) right across the 5 volt power inputs (pins 9,13) of the gate driver chips. It is also a good idea to do the same with the V-Gate voltage inputs (pins 3,2). With the large motor currents that this circuit can drive, a 4700microfarad electrolytic cap was put between the + battery voltage and ground right next to the transistors on the A side. Large wire (#12) was used to distribute the + battery voltage and ground around the FET's. A fuse should be used between the battery pack and this speed controller because of the large amounts of current that Nicad Batteries can supply. Running this circuit without a fuse in an invitation to a fire!

The gate outputs of U11 drive the FET gates through 30 Ohm resistors to prevent oscillations. The FET's chosen (IRFP064) were chosen for their large current handling abilities (about 70 Amps), low on resistance (0.009 Ohms) and I had some already. If you have some other N Channel FET's that will handle the voltage and current you want to drive, there should not be a problem swapping them.

The shutdown inputs of all of the gate drivers are tied together and connected to the jumper block (J7) with the output of the comparator (U6-B) in the No-Signal safety shutdown circuit. Jumper block J7 allows the FET drivers to be always enabled, always disabled or controlled by the No-Signal safety shutdown circuit. **For the initial testing, calibration and setup process it is extremely important to turn off the outputs so that tuning can be done without having strange and unpredictable stuff happen to the outputs.** Note that you disable the FET drivers by tying the shutdown input high to 5 volts.

2.5 Power Supplies

There are two separate power supplies in this circuit, a 5 volt supply for the control circuitry and optionally the radio control receiver, and the 18 volt gate drive voltage.

Details: The 5 volt regulator chosen is an LM2937ET-5. It is a low dropout type linear regulator which will allow the battery voltage to drop below 6 volts before it stops operating. It will handle 500 mA of current (this controller needs less than 100mA) and accepts input voltages up to 26 volts. If battery voltages above 7.2 volts are used, or if this regulator runs a servo or two in addition to the radio, a heat sink would be a good idea for the regulator. Be sure to use a tantalum or low ESR electrolytic capacitor on the output of this regulator and mount them physically close to the regulator.

The 18 volt regulator is a small switchmode boost converter built with a Motorola MC34163P IC. It supplies very little current, but converts the 7.2 volts from the battery up to 18 volts for the gate drive circuits. There is not much to be said about this circuit, it was lifted directly from Motorola's databook. The output current is less than 25 mA and might be as low as a few milliAmps in static conditions. The short circuit protection was set up to shut down at 150 mA.

3.0 Construction

The prototype was built on one perfboard with point to point wiring techniques. It was built one section at a time, testing each section upon completion. This approach makes troubleshooting much easier since it is not necessary to troubleshoot the entire board at once.

As mentioned earlier, large wire should be used in the power section. The battery leads should connect directly to the buss wires that distribute the battery voltage and grounds through the power section. The signal section has it's own ground and 5 Volt distribution, running above and below the components. The signal section's ground ties to the power section ground at the same point that the battery ground comes in. The battery voltage to the regulators should take off from the same point that the battery + ties to the buss wires.

All of the power FET's were put in two rows with high side in one row and the low side in the other row. Putting the driver IC's between the two rows allows very short gate wiring which is a good thing. The connections for the driver IC's to the FET Source leads should be kept short and go directly to the lead on the FET, to minimize parasitic inductance. Due to the high currents and fast switching rates present in the output section, keeping lead inductance low is ESSENTIAL!

After a lot of experimentation with several prototypes, I am starting to believe that it may not be possible to drive high current motors with a hand wired prototype. Original testing was done with small motors drawing 2 or 3 amps with no problems. Later on, higher current motors drawing 20 or 30 amps (standard RC car motors) were used. Early testing with the larger motors resulted in FET and driver IC failures in minutes of operation. Further testing led to reducing the dead time between switching the high and low side transistors in the output sections, adding zener diodes to protect the driver IC's and fast diodes to supplement the synchronous rectification. After these modifications, the reliability was greatly improved, but still not acceptable with large motors. The next step will be building a PC board and testing this approach.

Since the control sections of this circuit involve fairly low level analog signals, they should be built fairly close together and physically separated from the power section.

4.0 Modifications

As mentioned earlier, this controller can be built in a number of configurations.If this controller were to be set up for two joysticks, one for each motor like a bulldozer, most of sheet 3 can be deleted, with the exception of the No-Signal safety shutoff stuff. In this case, connect the SPEED-CTL-V signal to the CTL-V-1 input and the STEERING-CTL-V signal to the CTL-V-2 input on sheet 4.

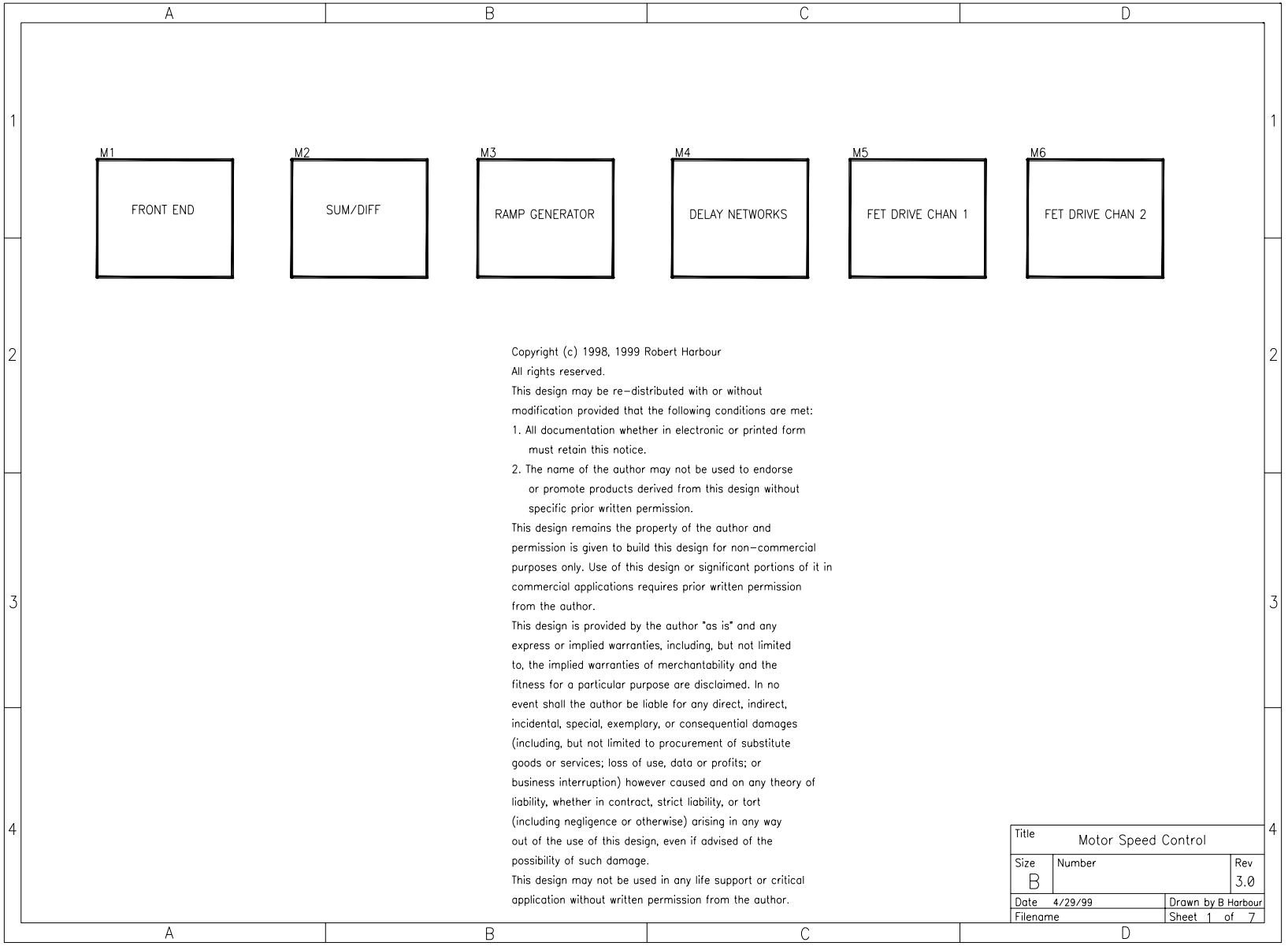
This circuit can be built easily as a direct wired system, saving a bunch of parts. The whole second page can be deleted and two pots used. The pots should be connected so that they put out about 2.5 volts when centered and should swing up and down about 1 volt from

there. The wipers of the pots would be connected to the SPEED-CTL-V and STEERING-CTL-V inputs on the third sheet of the schematic.

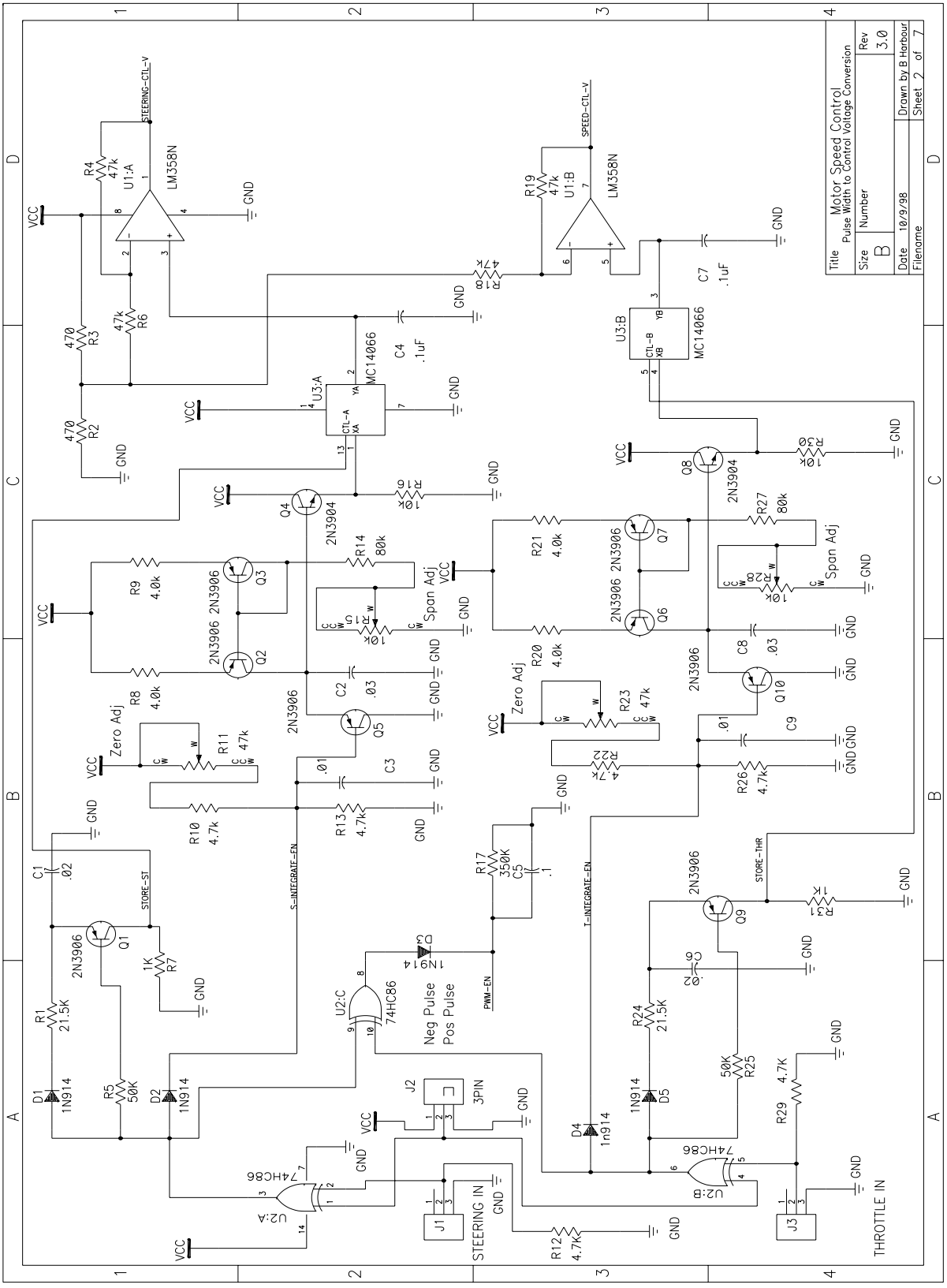
For direct connect bulldozer style controls, use the same pot arrangement described above, except route the pot wipers to the CTL-V-1 and CTL-V-2 inputs on sheet 4. In this mode, all of sheet 2 and 3 can be deleted.

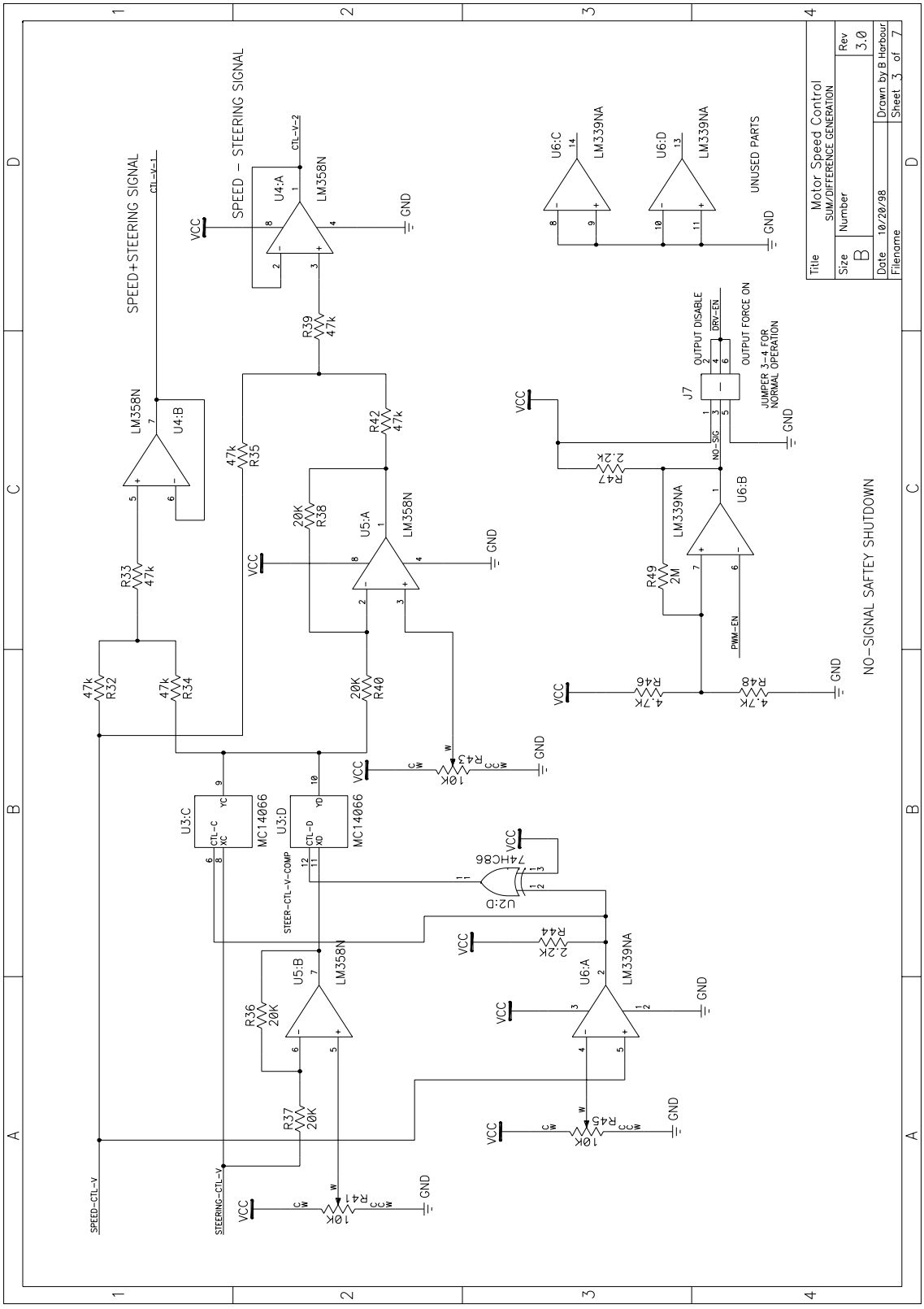
For direct wired applications, shielded cable should be used to keep noise out of the control voltages. Also, the No-Signal safety shutdown stuff can be deleted in a direct wired application, but the jumper block should be kept for tuning and testing.

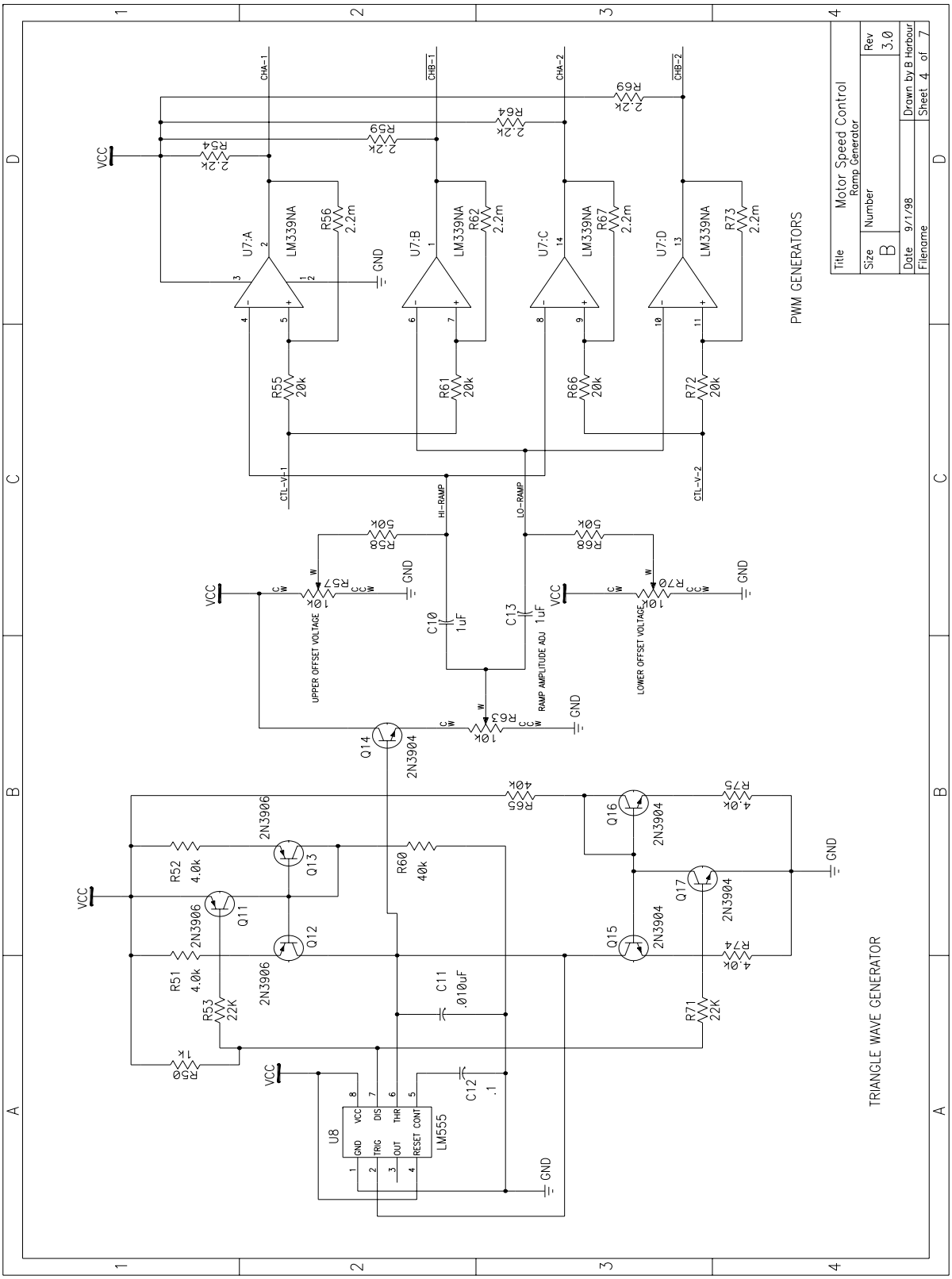
5.0 Schematic Diagrams

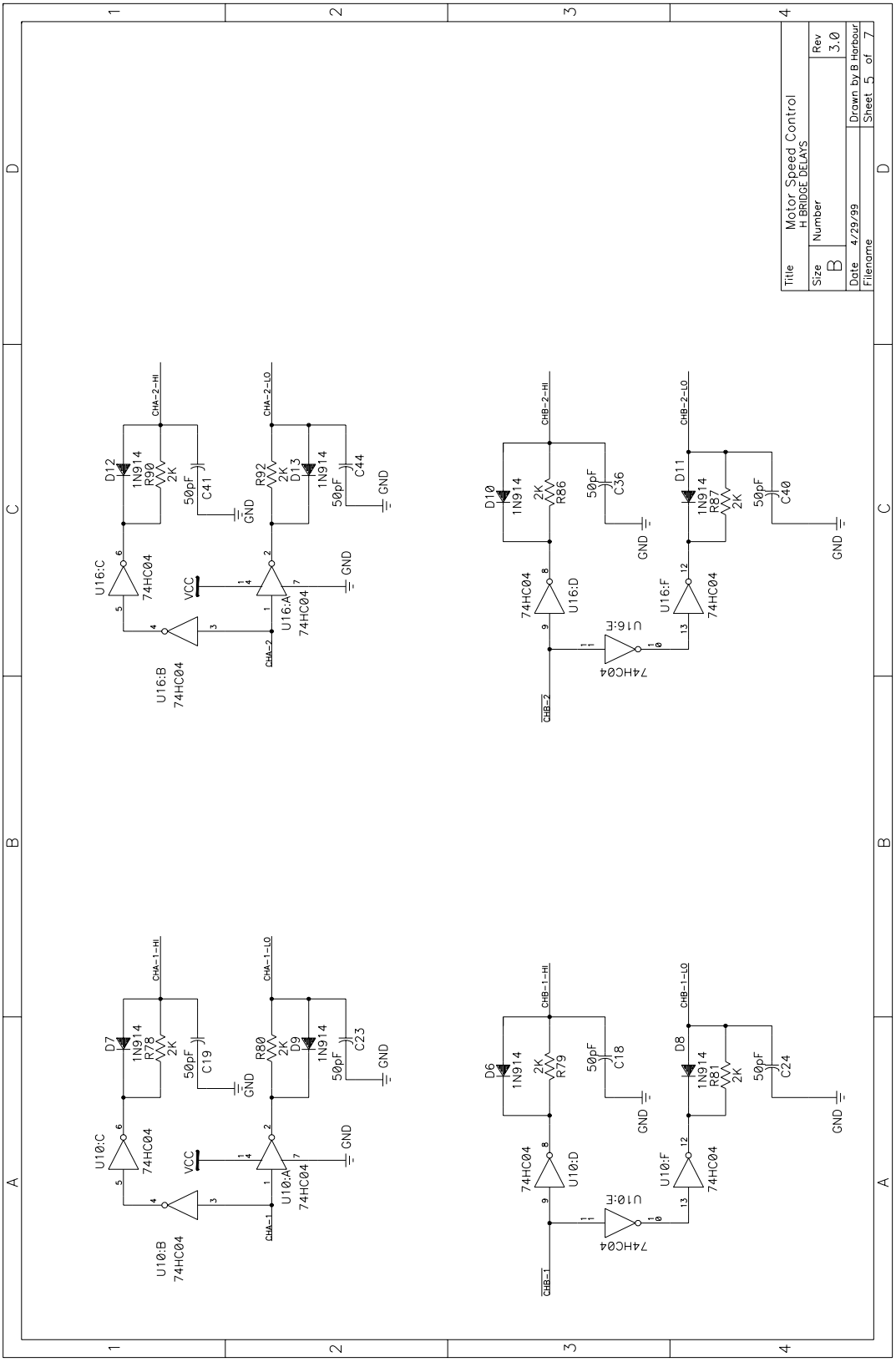


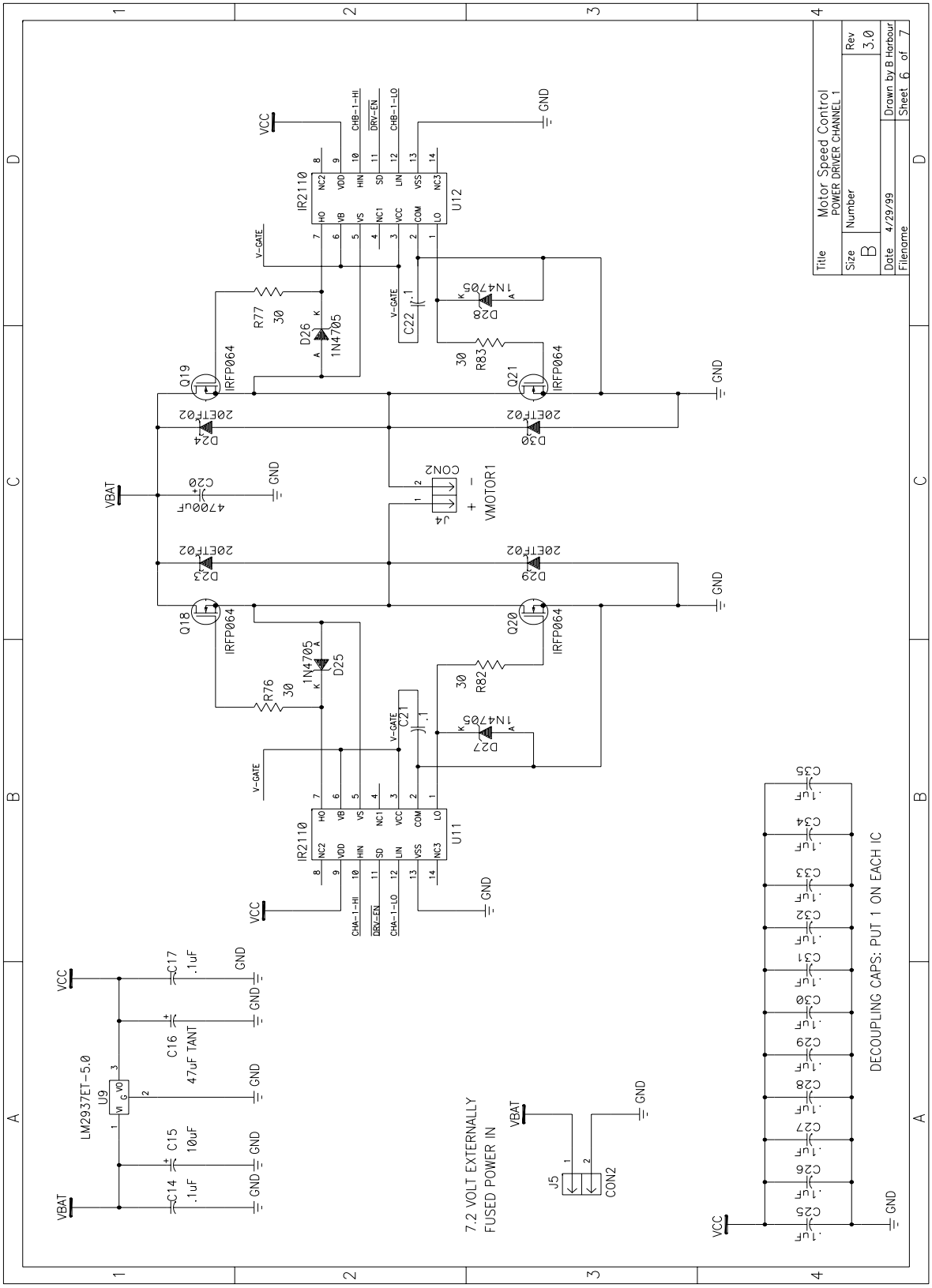
Title	Motor Speed Control	
Size B	Number	Rev 3.0
Date 4/29/99		Drawn by B Harbour
Filename		Sheet 1 of 7

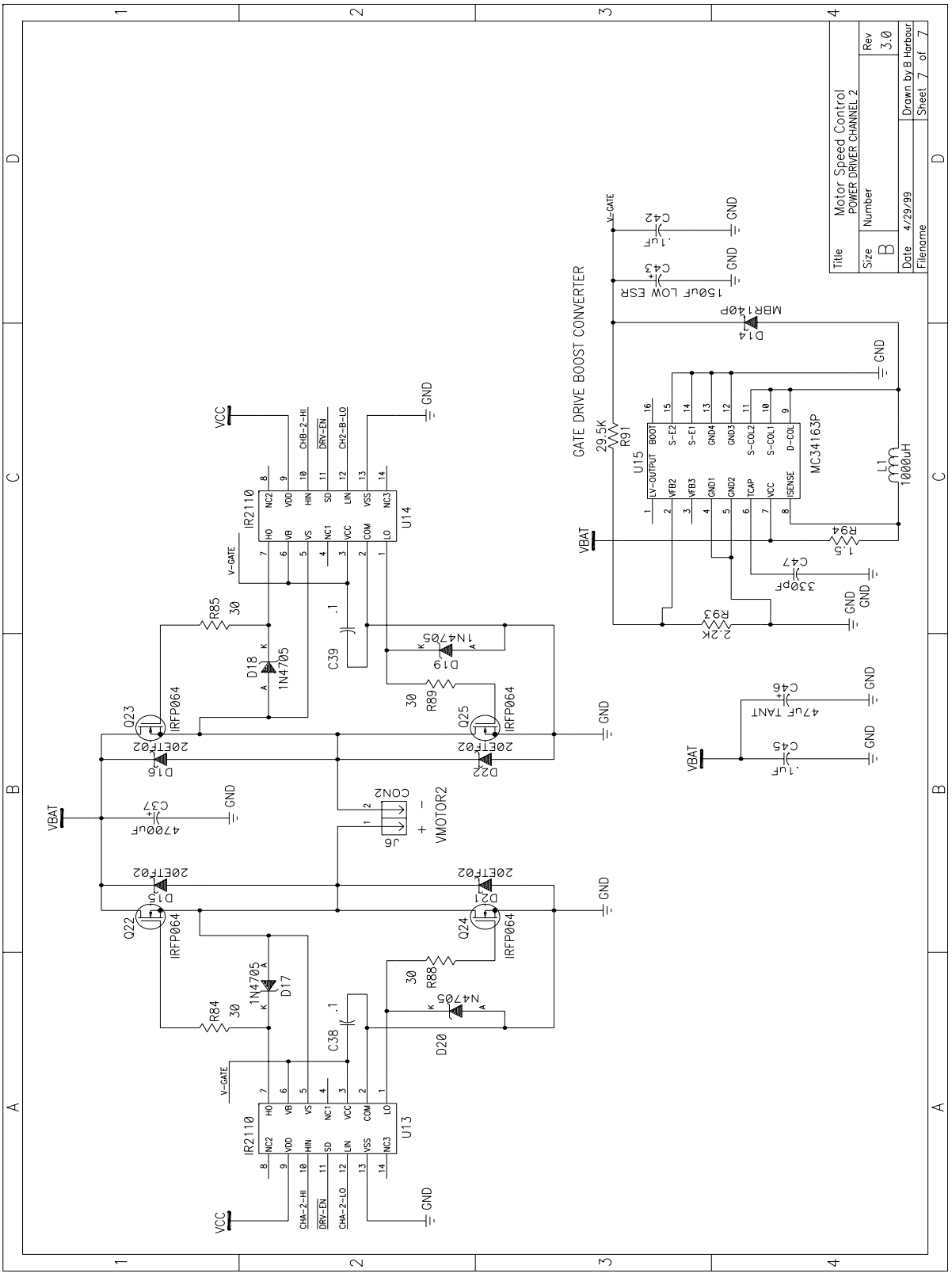

Motor Speed Control
Pulse Width to Control Voltage Conversion
Rev 3.0
Size B
Number
Date 10/9/98
Drawn by B Harbour
Filename
Sheet 2 of 7
STEERING-CTL-V
SPEED-CTL-V
LM358N
MC14066
2N3904
2N3906
74HC86
1N914
Span Adj
Zero Adj
Neg Pulse
Pos Pulse
S-INTEGRATE-EN
T-INTEGRATE-EN
PWM-EN
STORE-ST
STORE-THR
STEERING IN
THROTTLE IN
3PIN
VCC
GND


SPEED+STEERING SIGNAL
CTL-V-1
SPEED - STEERING SIGNAL
CTL-V-2
U4:A
LM358N
U4:B
LM358N
VCC
GND
R39
47k
R42
47k
47k
R35
R33
47k
47k
R32
47k
R34
20K
R38
20K
R40
U5:A
LM358N
U3:C
MC14066
U3:D
MC14066
CTL-C
XC
YC
CTL-D
XD
YD
STEER-CTL-V-COMP
U2:D
74HC86
R43
10K
U5:B
LM358N
R36
20K
R37
20K
R41
10K
U6:A
LM339NA
R44
2.2K
R45
10K
SPEED-CTL-V
STEERING-CTL-V
U6:C
LM339NA
U6:D
LM339NA
UNUSED PARTS
J7
OUTPUT DISABLE
DRV-EN
OUTPUT FORCE ON
JUMPER 3-4 FOR
NORMAL OPERATION
NO-SIG
R47
2.2K
U6:B
LM339NA
R49
2M
R46
4.7K
R48
4.7K
PWM-EN
NO-SIGNAL SAFTEY SHUTDOWN
Title
Motor Speed Control
SUM/DIFFERENCE GENERATION
Size
B
Number
Rev
3.0
Date
10/28/98
Drawn by B Harbour
Filename
Sheet 3 of 7


Motor Speed Control
Ramp Generator
Rev 3.0
Number
Size B
Date 9/1/98
Drawn by B Harbour
Filename
Sheet 4 of 7
PWM GENERATORS
TRIANGLE WAVE GENERATOR
CHA-1
CHB-1
CHA-2
CHB-2
VCC
GND
U7:A
U7:B
U7:C
U7:D
LM339NA
R56 2.2m
R62 2.2m
R67 2.2m
R73 2.2m
R54 2.2k
R59 2.2k
R64 2.2k
R69 2.2k
R55 20k
R61 20k
R66 20k
R72 20k
CTL-V-1
CTL-V-2
HI-RAMP
LO-RAMP
R58 50k
R68 50k
R57 10k
R70 10k
UPPER OFFSET VOLTAGE
LOWER OFFSET VOLTAGE
C10 1uF
C13 1uF
R63 10k
RAMP AMPLITUDE ADJ
Q14 2N3904
R65 40k
R75 4.0k
Q16 2N3904
Q17 2N3904
Q15 2N3904
Q13 2N3906
Q11 2N3906
Q12 2N3906
R52 4.0k
R51 4.0k
R60 40k
R53 22K
R71 22K
C11 .010uF
R50 1k
C12 .1
U8 LM555
GND TRIG OUT RESET CONT THR DIS VCC


Title
Motor Speed Control
H BRIDGE DELAYS
Size
B
Number
Rev
3.0
Date 4/29/99
Drawn by B Hardsour
Filename
Sheet 5 of 7
CHA-2-HI
CHA-2-LO
CHA-1-HI
CHA-1-LO
CHB-2-HI
CHB-2-LO
CHB-1-HI
CHB-1-LO
D12
D13
D7
D9
D10
D11
D6
D8
1N914
R90
R92
R78
R80
R86
R87
R79
R81
2K
50pF
C41
C44
C19
C23
C36
C40
C18
C24
GND
VCC
U16:C
U16:B
U16:A
U16:D
U16:F
U16:E
U10:C
U10:B
U10:A
U10:D
U10:F
U10:E
74HC04
CHA-2
CHA-1
CHB-2
CHB-1


Motor Speed Control
POWER DRIVER CHANNEL 1
Rev 3.0
Number
Date 4/29/99
Drawn by B Harbour
Filename
Sheet 6 of 7
U11
U12
IR2110
IRFP064
20ETF02
1N4705
1N4705
LM2937ET-5.0
U9
R76
R77
R82
R83
C21
C22
C20
C17
C16
C15
C14
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
CON2
J4
J5
VMOTOR1
VBAT
VCC
GND
V-GATE
CHA-1-HI
CHA-1-LO
CHB-1-HI
CHB-1-LO
DRV-EN
7.2 VOLT EXTERNALLY FUSED POWER IN
DECOUPLING CAPS: PUT 1 ON EACH IC


Motor Speed Control
POWER DRIVER CHANNEL 2
Rev 3.0
Size B
Number
Date 4/29/99
Drawn by B Harbour
Filename
Sheet 7 of 7
GATE DRIVE BOOST CONVERTER
MC34163P
U15
IR2110
U13
U14
IRFP064
20ETF02
1N4705
1N4705
MBR140P
150uF LOW ESR
1000uH
29.5K
R91
2.2K
R93
.5
R94
330pF
C47
47UF TANT
C46
.1uF
C45
4700uF
C37
.1uF
C42
.1uF
C43
.1
C38
.1
C39
30
R84
30
R85
30
R88
30
R89
VBAT
VCC
GND
V-GATE
VMOTOR2
CON2
CHA-2-HI
DRV-EN
CHA-2-LO
CHB-2-HI
DRV-EN
CH2-B-LO

5.1 Parts List

Bill of Materials SP_CTL.S01

Speed Control BOM

Quantity	Type	Value	Ref Designators
2	POT	47k	R11,R23
1	RES	1.5	R94
2	RES	10k	R16,R30
3	RES	1K	R7,R31,R50
7	RES	2.2k	R44,R93,R47,R54,R59,R64, R69
4	RES	2.2m	R56,R62,R67,R73
8	RES	20k	R36,R37,R38,R40,R55,R61,R66,R72
2	RES	21.5K	R1,R24
2	RES	22K	R53,R71
1	RES	29.5K	R91
8	RES	2K	R78,R79,R80,R81,R86,R87,R90,R92
1	RES	2M	R49
8	RES	30	R76,R77,R82,R83,R84,R85,R88,R89
1	RES	350K	R17
8	RES	4.0k	R8,R9,R20,R21,R51,R52,R74,R75
8	RES	4.7k	R12,R29,R46,R48,R10,R13,R22,R26
2	RES	40k	R60,R65
2	RES	470	R2,R3
10	RES	47k	R4,R6,R18,R19,R32,R33,R34,R35,R39,R42
4	RES	50K	R5,R25,R58,R68

2	RES	80k	R14,R27
8	POT	10k 10 Turn	R41,R43,R45,R15,R28,R57,R63,R70
2	CAP	.01uF	C3,C9
1	CAP	.010uF	C11
2	CAP	.02uF	C1,C6
2	CAP	.03uF Styrene	C2,C8
6	CAP	.1uF	C5,C12,C21,C22,C38,C39,C4,C7, C14,C17,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C42,C45
2	CAP	1uF	C10,C13
1	CAP	330pF	C47
8	CAP	50pF	C18,C19,C23,C24,C36,C40,C41,C44
1	POLCAP	10uF	C15
1	POLCAP	150uF LOW ESR	C43
2	POLCAP	4700uF	C20,C37
2	POLCAP	47uF TANT	C16,C46
3	3PIN	.1 Male Pins	J1,J2,J3
3	CON2	Power Connectors	J4,J5,J6
1	JMP3X2	.1 3X2 Jumper Pins	J7
1	IND	1000uH 100mA	L1
13	DIODE	1N914	D1,D2,D3,D5,D6,D7,D8,D9, D10,D11,D12,D13,D4
8	DIODE-220	20ETF02	D15,D16,D21,D22,D23,D24,D29,D30
1	DIODE-SCHOTKY	MBR140P	D14

8	ZENER	1N4705	D17,D18,D19,D25,D26,D27,D20,D28
2	74HC04	Hex Inverter	U10,U16
1	74HC86	Quad EXOR Gate	U2
4	IR2110	FET Gate Driver	U11,U12,U13,U14
1	LM2937ET-5.0	LDO 5V Regulator	U9
2	LM339NA	Quad Comparator	U6,U7
3	LM358N	Dual Op Amp	U1,U4,U5
1	LM555	Timer IC	U8
1	MC14066	Quad Analog Switch	U3
1	MC34163P	Switching Regulator	U15
8	MOSFETN	IRFP064	Q18,Q19,Q20,Q21,Q22,Q23, Q24,Q25
6	NPN	2N3904	Q4,Q8,Q14,Q15,Q16,Q17
11	PNP	2N3906	Q1,Q2,Q3,Q5,Q6,Q7,Q9,Q10, Q11,Q12,Q13

Total Parts: 220