Tutorial Outline

8:30 - 8:45	Introduction and motivation
8:45 - 9:05	Sources of power in CMOS designs
9:05 - 9:30	Power analysis tools and techniques
9:30 - 10:30	Gate & functional unit design issues & techniques
10:30 - 10:50	BREAK
10:50 - 12:15	Architectural level issues and techniques
12:15 - 1:30	LUNCH
1:30 - 2:30	Low power memory system design
2:30 - 3:30	Software level issues and techniques
3:30 - 3:50	BREAK
3:50 - 4:30	Software level issues and techniques, con't
4:30 - 4:45	Future challenges

Where Does Power Go in CMOS?

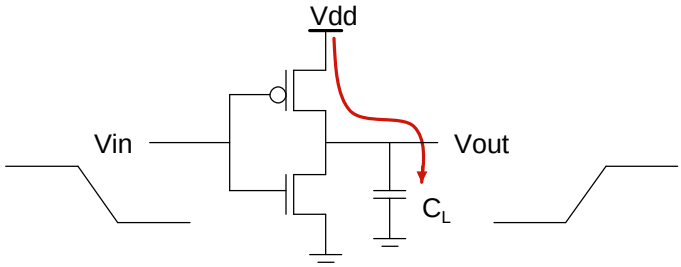
- Dynamic Power Consumption
  - » charging and discharging capacitors
- Short Circuit Currents
  - » short circuit path between supply rails during switching
- Leakage Current
  - » leaking diodes and transistors
- Static Currents
  - » design styles such as pseudo NMOS

CMOS Gate Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\to1} + t_{sc} V_{DD} I_{peak} P_{0\to1} + V_{DD} I_{leakage}$$

$$P = C_L V_{DD}^2 f_{0\to1} + t_{sc} V_{DD} I_{peak} f_{0\to1} + V_{DD} I_{leakage}$$

Dynamic Power Consumption



Energy/transition = $C_L * V_{DD}^2 * P_{0\to1}$

Power = Energy/transition * f = $C_L * V_{DD}^2 * P_{0\to1} * f$ ($f_{0\to1}$)

Not a function of transistor sizes!
Data dependent - a function of switching activity!

Lowering Dynamic Power

- Reducing V_{DD} has a quadratic effect!
  - » Has a negative effect on performance especially as V_{DD} approaches $2V_T$
- Lowering C_L
  - » Improves performance as well
  - » Keep transistors minimum size (keeps intrinsic capacitance (gate and diffusion) small)
  - » Transistors should be sized only when C_L is dominated by extrinsic capacitance (fanout and wires)
- Reducing the switching activity, $f_{0\rightarrow1} = P_{0\rightarrow1} * f$
  - » A function of signal statistics and clock rate
  - » Impacted by logic and architecture design decisions

Dynamic Power Consumption is Data Dependent

Static 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$P_{A=1} = 1/2$

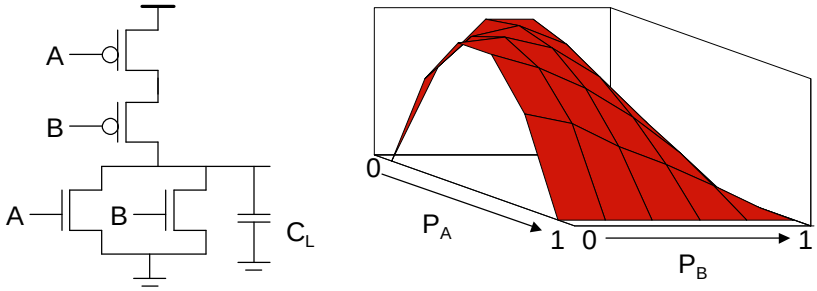
$P_{B=1} = 1/2$

Then transition probability

$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$

$= 3/4 \times 1/4 = 3/16$

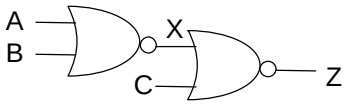
NOR Gate Transition Probabilities

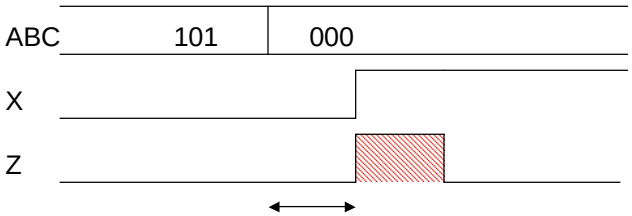


$$P_{0\to1} = P_0 \times P_1 = (1-(1-P_A)(1-P_B))(1-P_A)(1-P_B)$$

$P_{0\to1}$ is a strong function of signal statistics

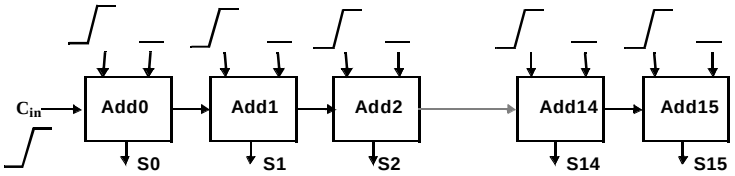
Glitching in Static CMOS Networks

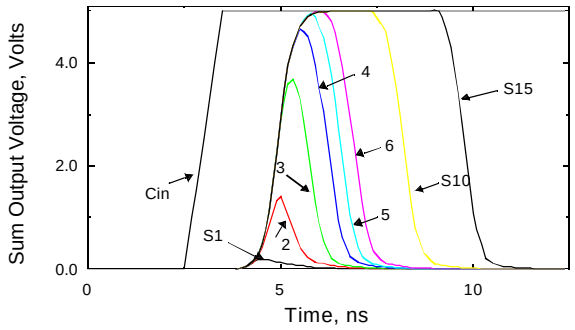




Unit Delay

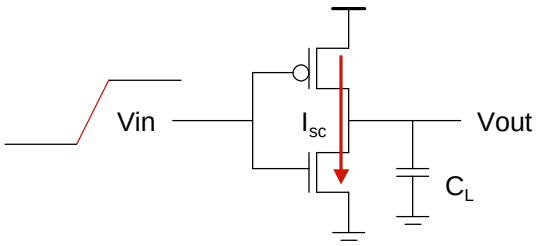
Glitching in an RCA





From Rabaey, 1995

Short Circuit Power Consumption



Finite slope of the input signal causes a direct current path between V_{DD} and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

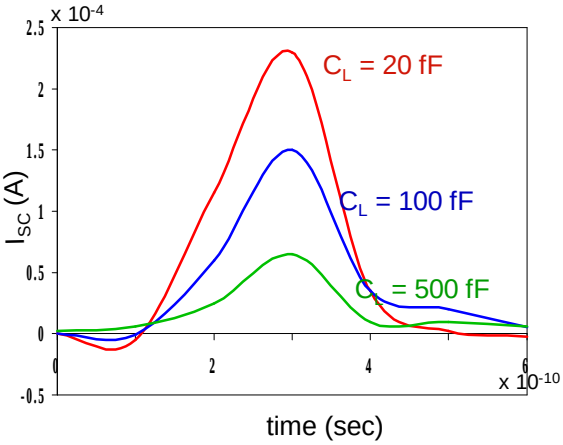
Short Circuit Currents Determinates

$$E_{sc} = t_{sc}\ V_{DD}\ I_{peak}\ P_{0\rightarrow1}$$

$$P_{sc} = t_{sc}\ V_{DD}\ I_{peak}\ f_{0\rightarrow1}$$

- Duration and slope of the input signal, t_{sc}
- I_{peak} determined by
  - » the saturation current of the P and N transistors which depend on their sizes, process technology, temperature, etc.
  - » the ratio between input and output slopes
    - – function of C_L

I_{SC} as a Function of C_L

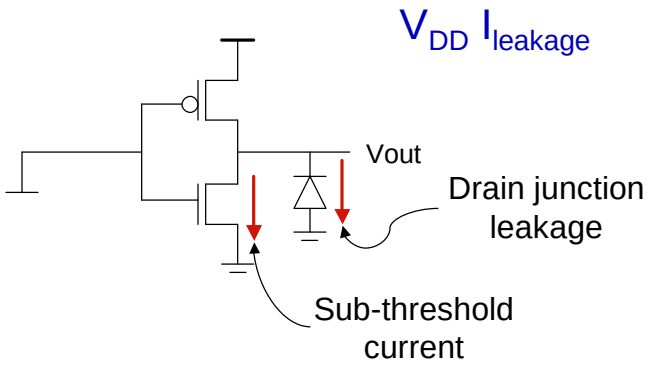


500 psec input slope

When load capacitance is small, power is dominated by I_{sc}.

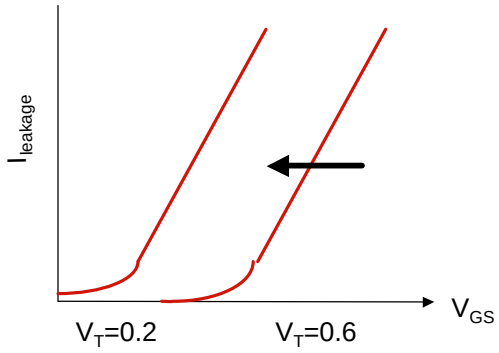
Short circuit dissipation is minimized by matching the rise/fall times of the input and output signals - slope engineering.

Leakage Power



Sub-threshold current is the dominant factor.
Increases exponentially with temperature!

Sub-Threshold in MOS



Continued scaling of supply voltage will make subthreshold conduction a dominate source of power dissipation.

Basic Principles of Low Power Design

$$P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} f_{0\rightarrow1} + V_{DD} I_{leakage}$$

- Reduce switching (supply) voltage
  - » quadratic effect -> dramatic savings
  - » negative effect on performance
- Reduce capacitance
- Reduce switching frequency
  - » switching activity
  - » clock rate
- Reduce glitching
- Reduce short circuit currents (slope engineering)
- Reduce leakage currents